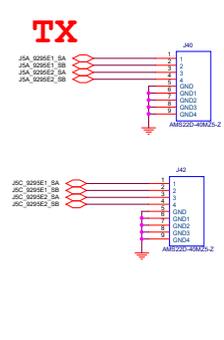
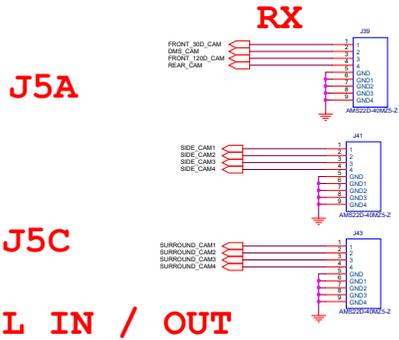


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		2			19
		3			20
		4			21
		5			22
		6			23
		7			24
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		17			



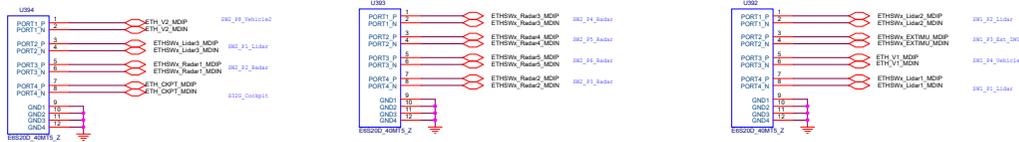




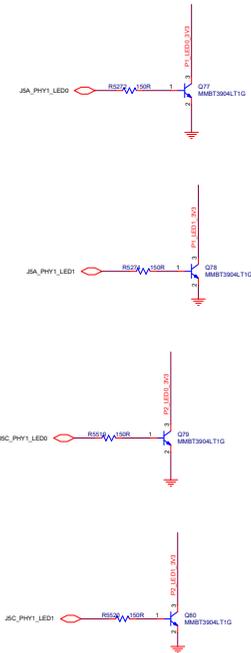
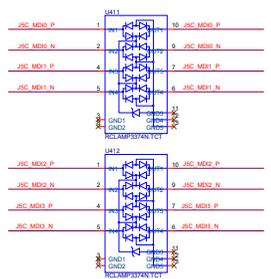
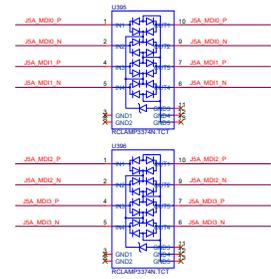
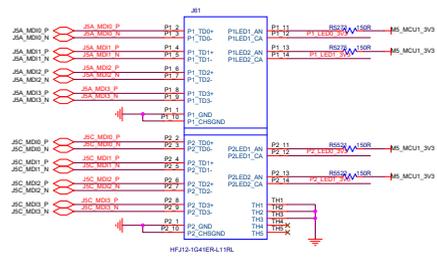


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100M/1000M-T1**

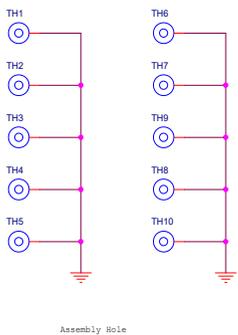


Signal map could swap

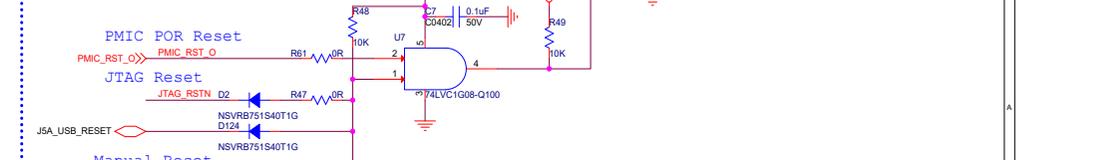
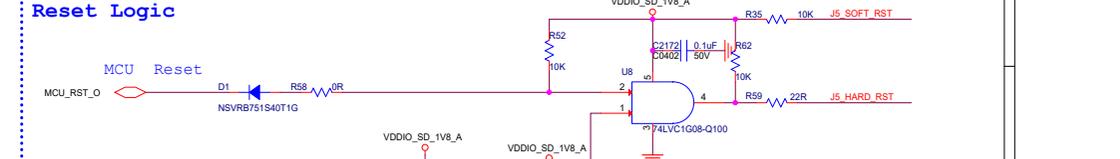
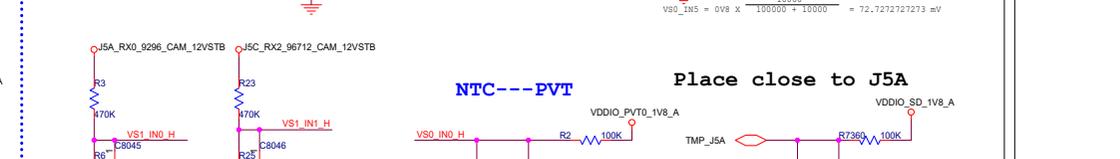
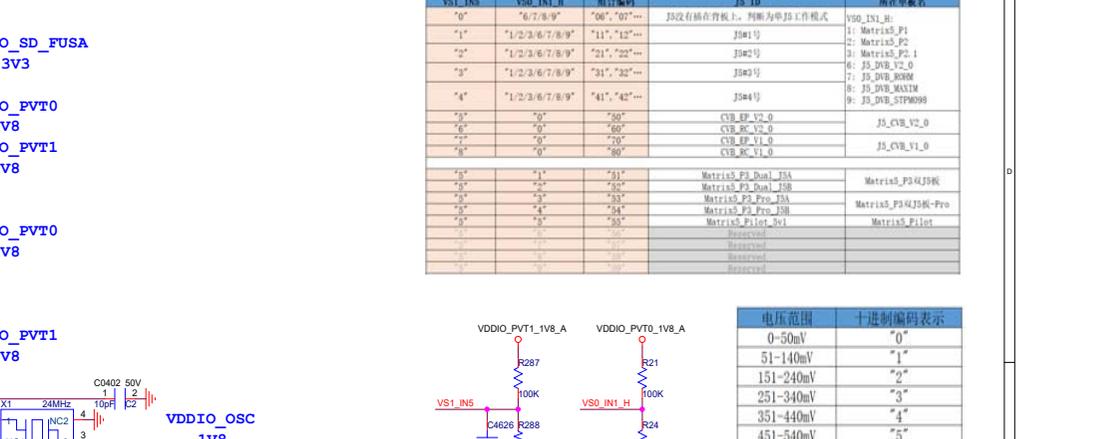
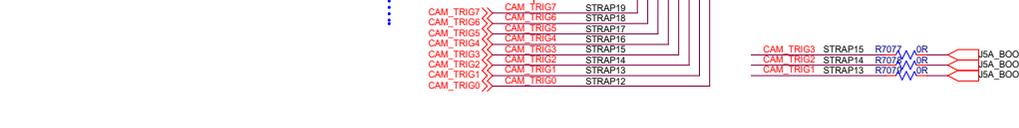
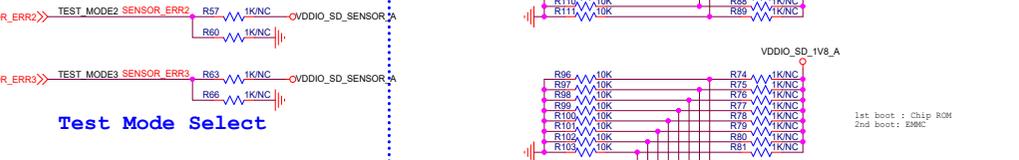
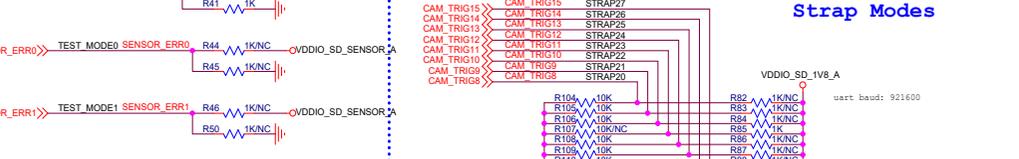
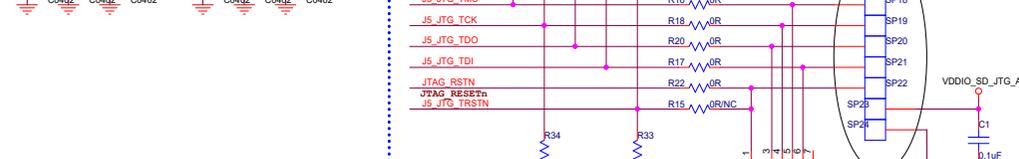
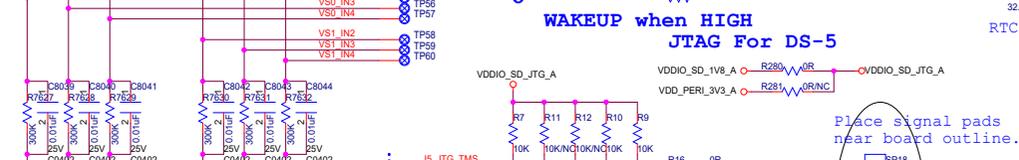
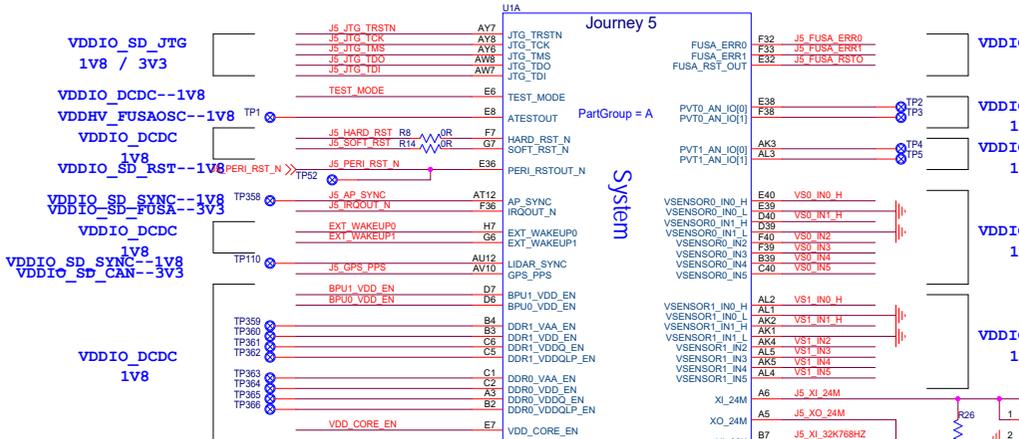




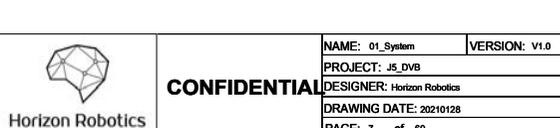
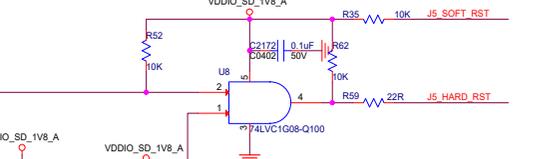
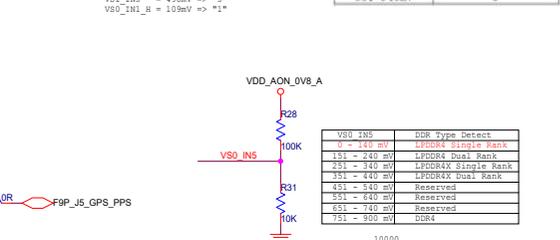
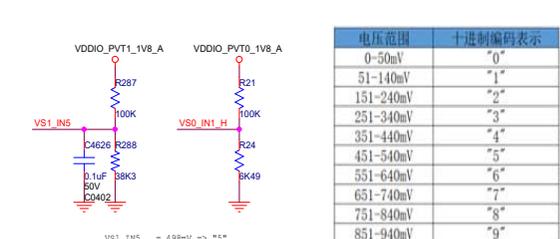
**MECH**



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Project: <Title>	Rev: <Rev Code>
Designer:	
Date: Wednesday, April 27, 2022	
Sheet: 6	of 68



VS1_INx	VS0_IN1_H	组合编码	J5_ID	所在单板名称
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"2"	"1/2/3/4/7/8/9"	"21", "22"	J3#2	2: Matrix5_P2
"3"	"1/2/3/4/7/8/9"	"31", "32"	J3#3	3: Matrix5_P3
"4"	"1/2/3/4/7/8/9"	"41", "42"	J3#4	4: Matrix5_P4
"5"	"0"	"50"	CVB_EP_V2_0	5: Matrix5_P5
"6"	"0"	"60"	CVB_EC_V2_0	6: JS_DVB_V2_0
"7"	"0"	"70"	CVB_EP_V1_0	7: JS_DVB_R00M
"8"	"0"	"80"	CVB_EC_V1_0	8: JS_DVB_MAXIM
"9"	"0"	"90"	CVB_EC_V1_0	9: JS_DVB_STP4098
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"100"	"0"	"1000"	Reserved	Reserved



Horizon Robotics

NAME: 01\_System | VERSION: v1.0

PROJECT: JS\_DVB

DESIGNER: Horizon Robotics

DRAWING DATE: 20210128

PAGE: 7 of 69

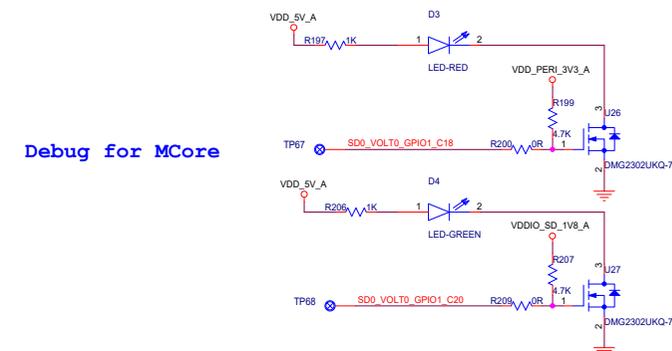
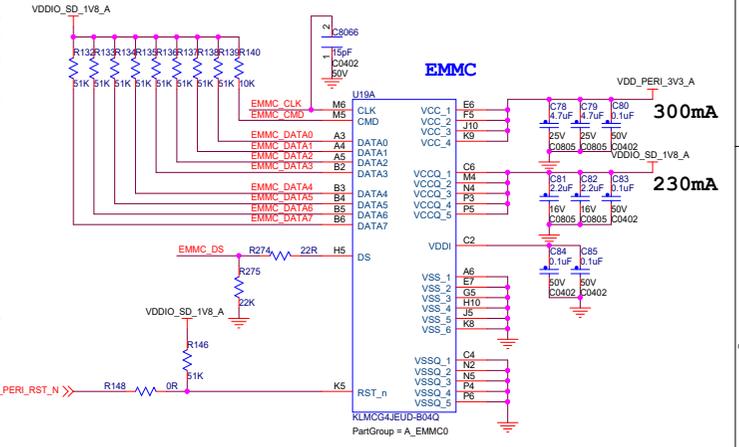
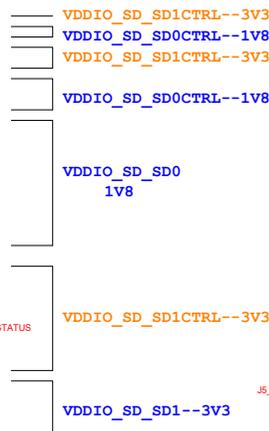
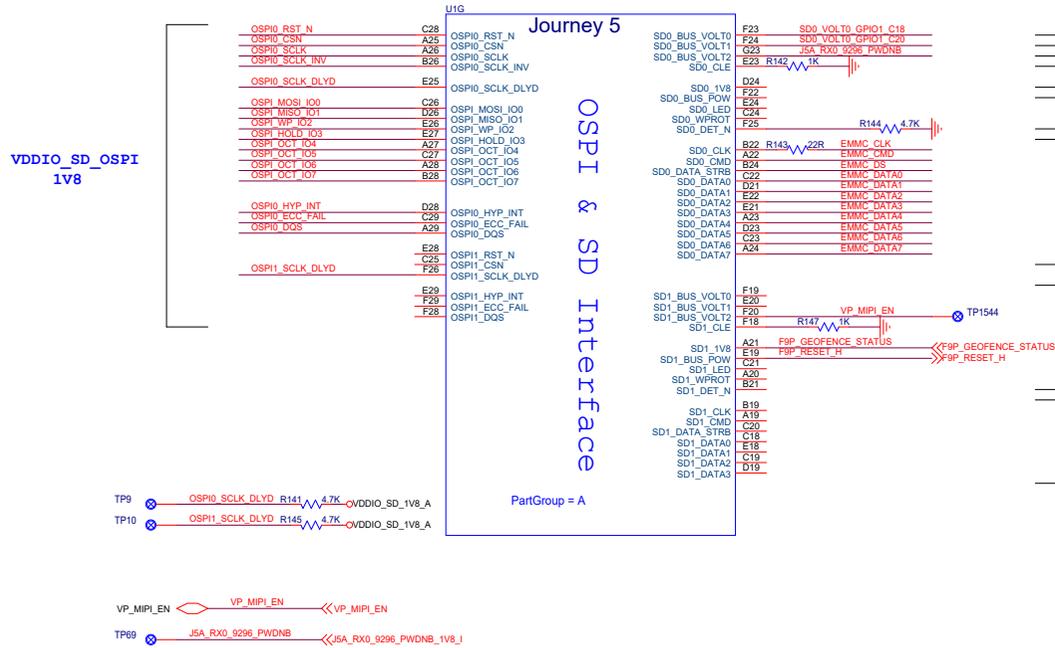




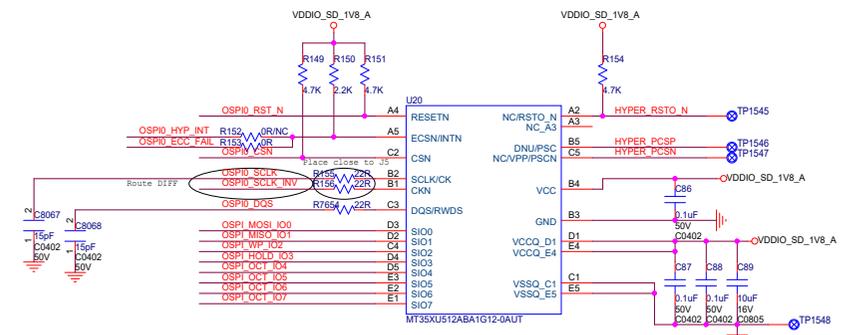
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 1 to switch on SD socket 3.3V supply, 0 to switch off the supply.

SD\_1V8: control PMIC:  
 1 -> enable to change VDDIO of SoC SDIO to 1.8V,  
 0-> VDDIO change back to default 3.3V.

SD\_BUS\_VOLT[0:2]: control PMIC,  
 select voltage level for VDDIO, maybe fixed to 3.0V or 3.3V



Hyper Flash



Xccela : 120mA  
 Hyper : 300mA



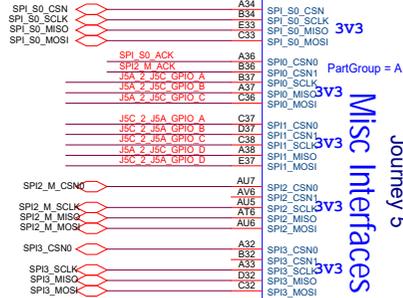
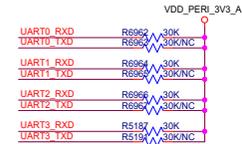
CONFIDENTIAL

NAME: 04_Bocd_flash	VERSION: v1.0
PROJECT: J5_DVB	
DESIGNER: Horizon Robotics	
DRAWING DATE: 20210128	
PAGE: 10 of 69	

VDDIO\_SD\_SPI2/3/S0/BIFSPI--3V3

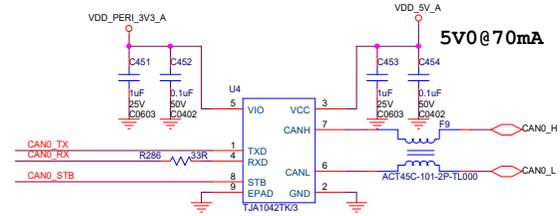
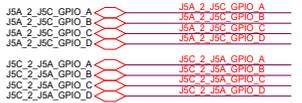
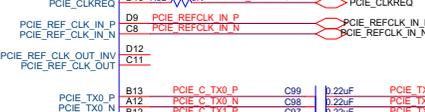
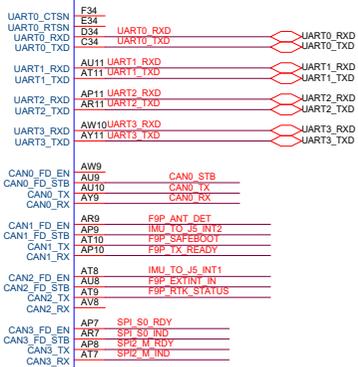
VDDIO\_SD\_SPI0/1--1V8

BIFSPI 1.8V



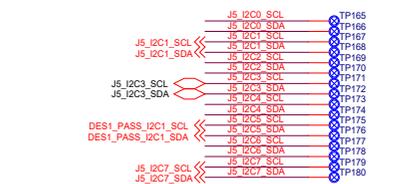
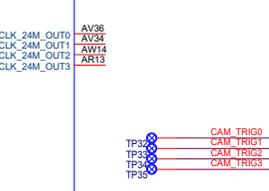
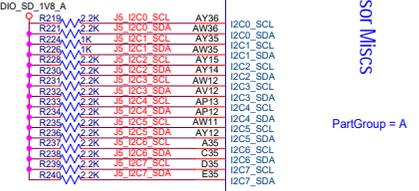
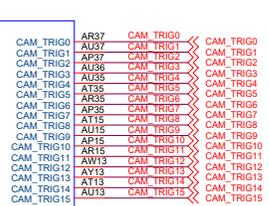
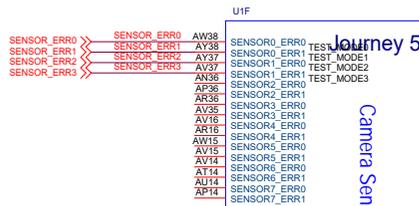
U1H  
 BIFSPI\_RSTN  
 BIFSPI\_SCLK  
 BIFSPI\_CS0  
 BIFSPI\_MISO  
 BIFSPI\_MOSI  
 SPI0\_CS0  
 SPI0\_SCLK  
 SPI0\_MISO  
 SPI0\_MOSI  
 SPI2\_M\_CS0  
 SPI2\_M\_SCLK  
 SPI2\_M\_MISO  
 SPI2\_M\_MOSI  
 SPI3\_CS0  
 SPI3\_SCLK  
 SPI3\_MISO  
 SPI3\_MOSI

PartGroup = A  
 Misc Interfaces  
 Journey 5



**CONFIDENTIAL**

NAME: 05_Ports	VERSION: v1.0
PROJECT: J5_DVB	
DESIGNER: Horizon Robotics	
DRAWING DATE: 20210128	
PAGE: 11 of 69	

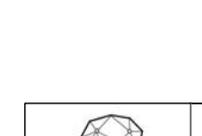
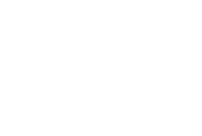
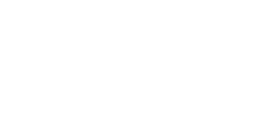
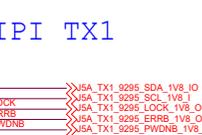
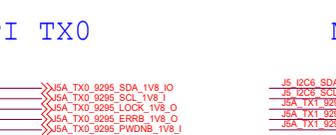
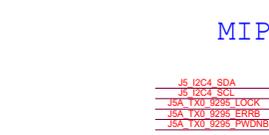
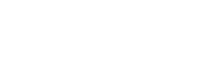
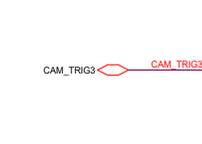
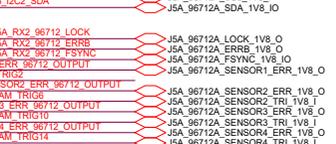
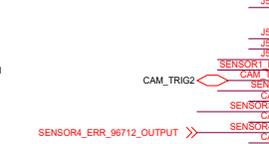


**MIPI RX0**

**MIPI RX1**

**MIPI RX2**

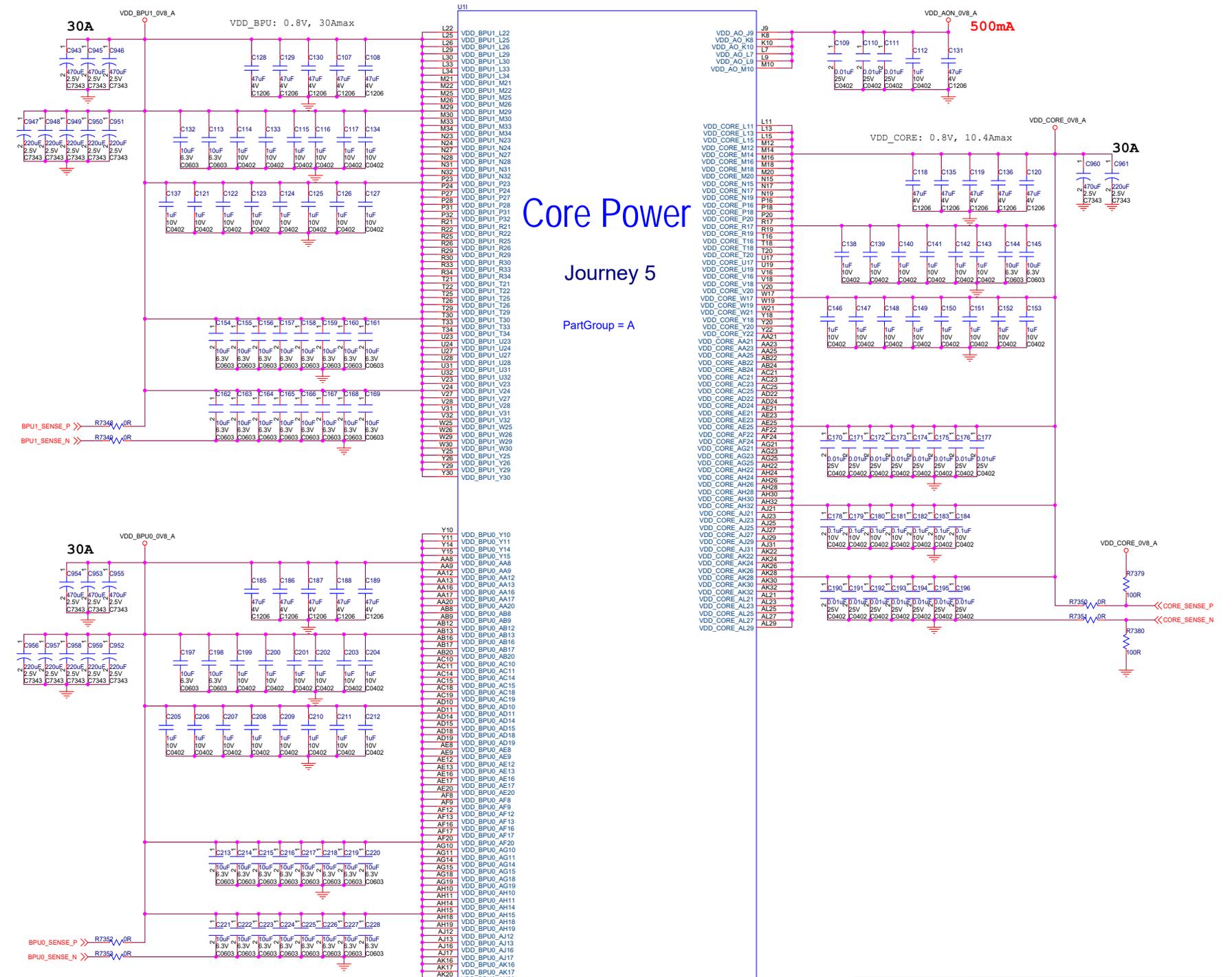
**MIPI RX3**



**CONFIDENTIAL**

NAME: 06_Ports_MIPI_RX_TX	VERSION: V1.0
PROJECT: J5_DVB	
DESIGNER: Horizon Robotics	
DRAWING DATE: 20210128	
PAGE: 12 of 69	





# Core Power

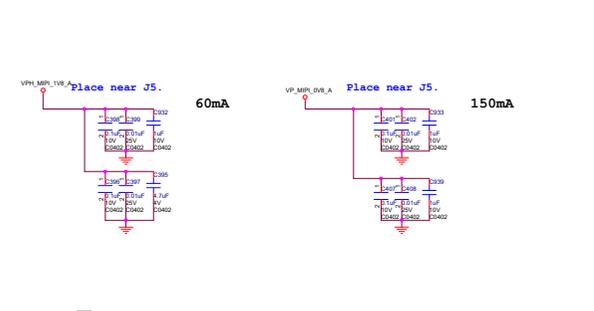
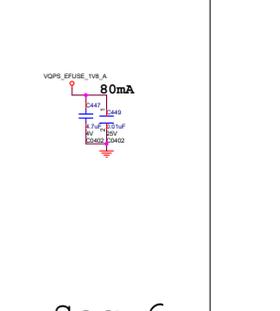
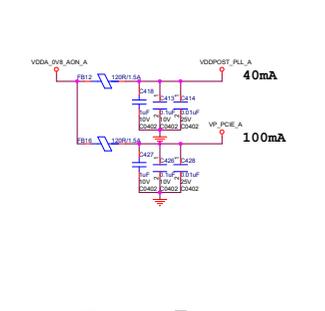
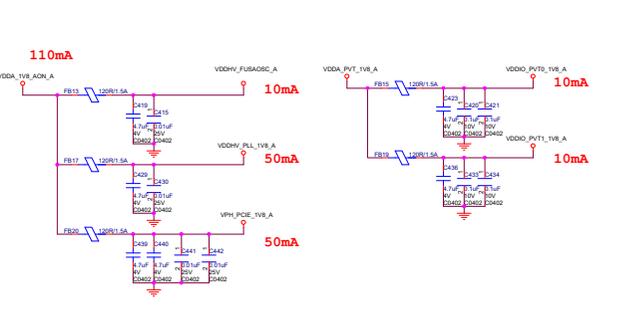
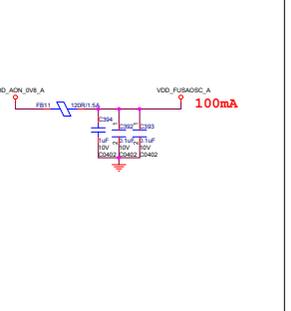
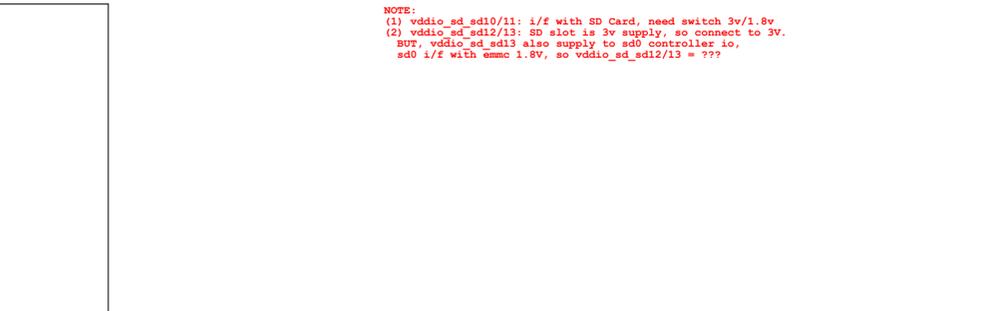
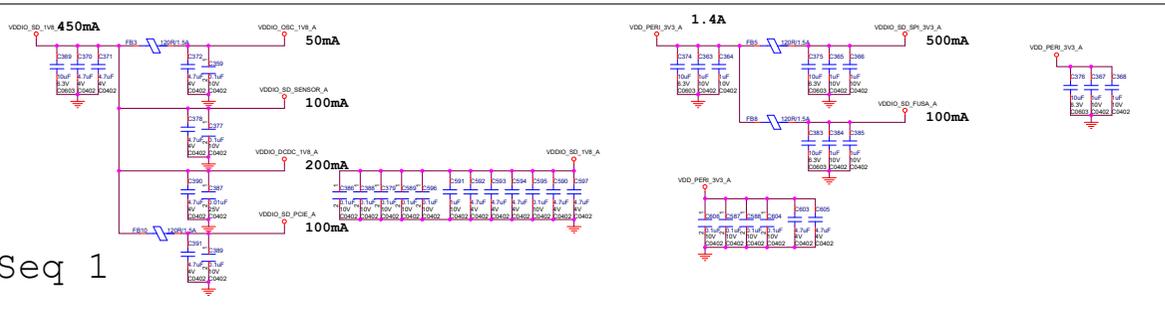
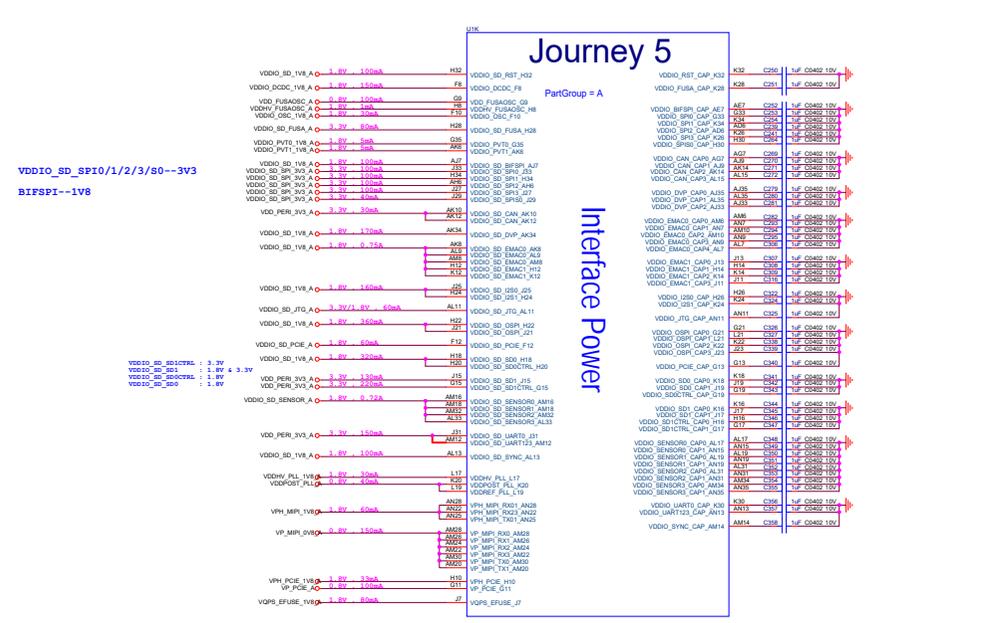
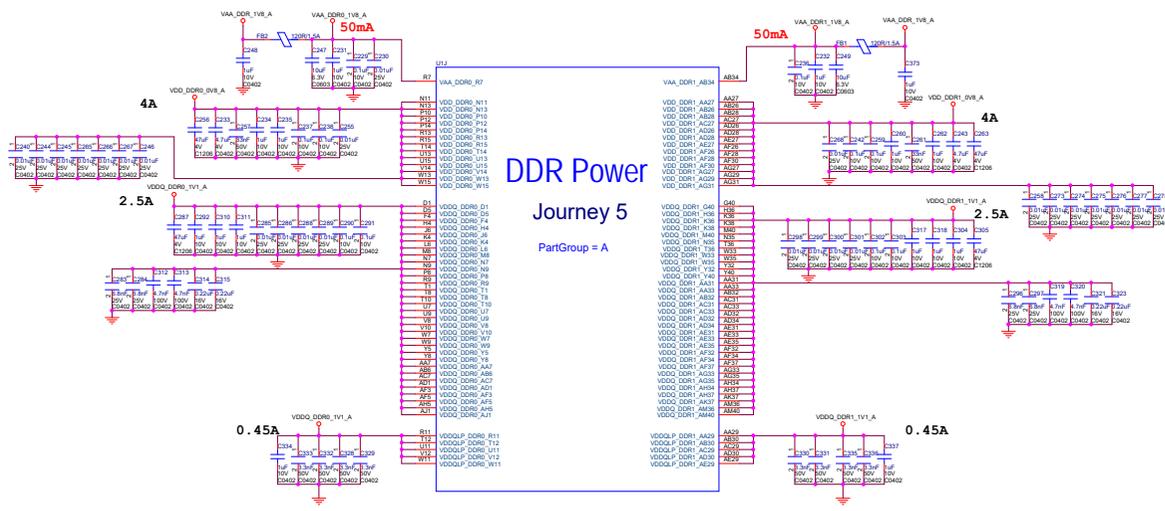
Journey 5

PartGroup = A



**CONFIDENTIAL**

NAME: 08_CORE_Power	VERSION: v1.0
PROJECT: J5_DVB	
DESIGNER: Horizon Robotics	
DRAWING DATE: 20210128	
PAGE: 14 of 69	



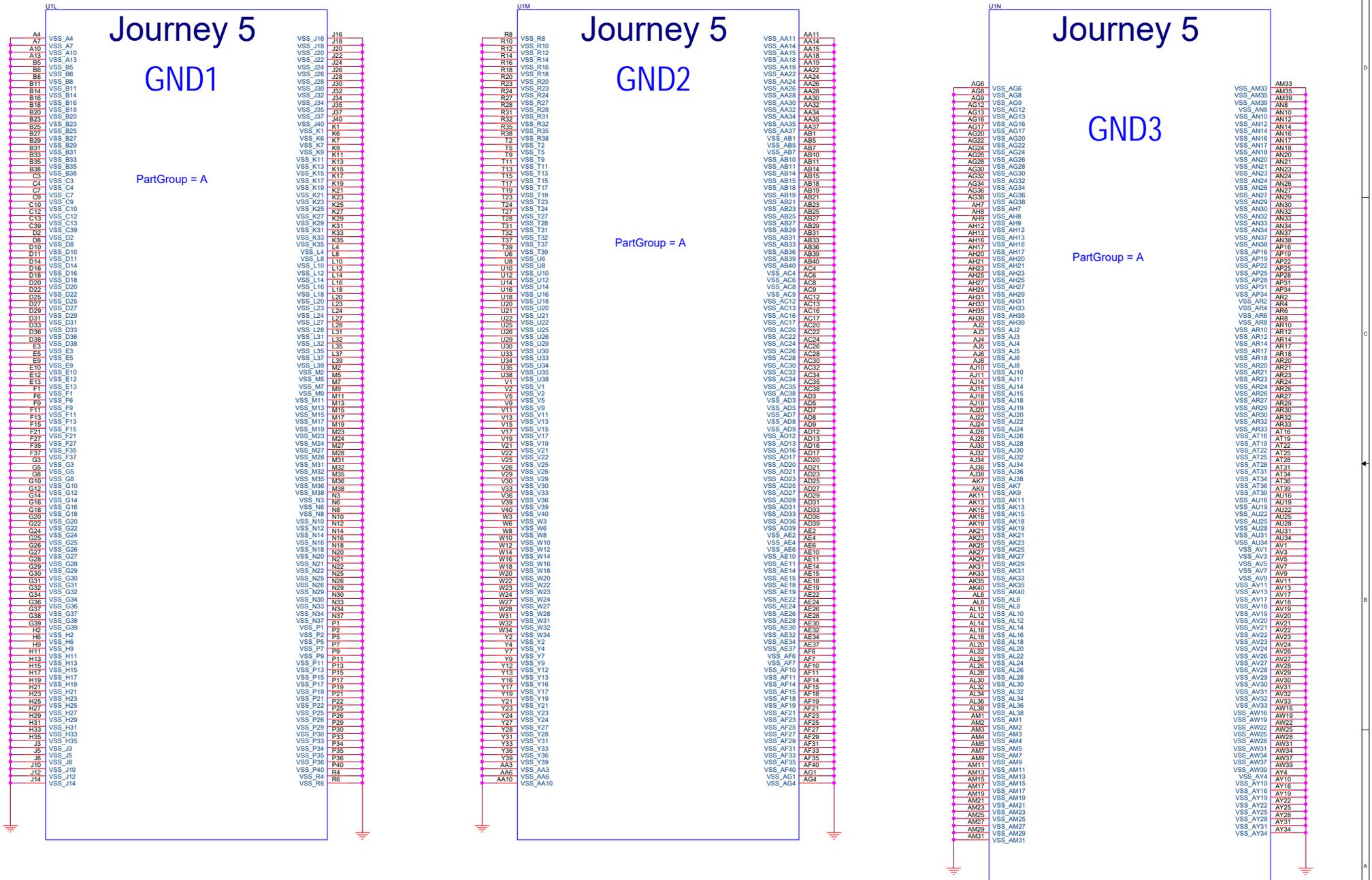
Seq 2

Seq 3

Seq 5

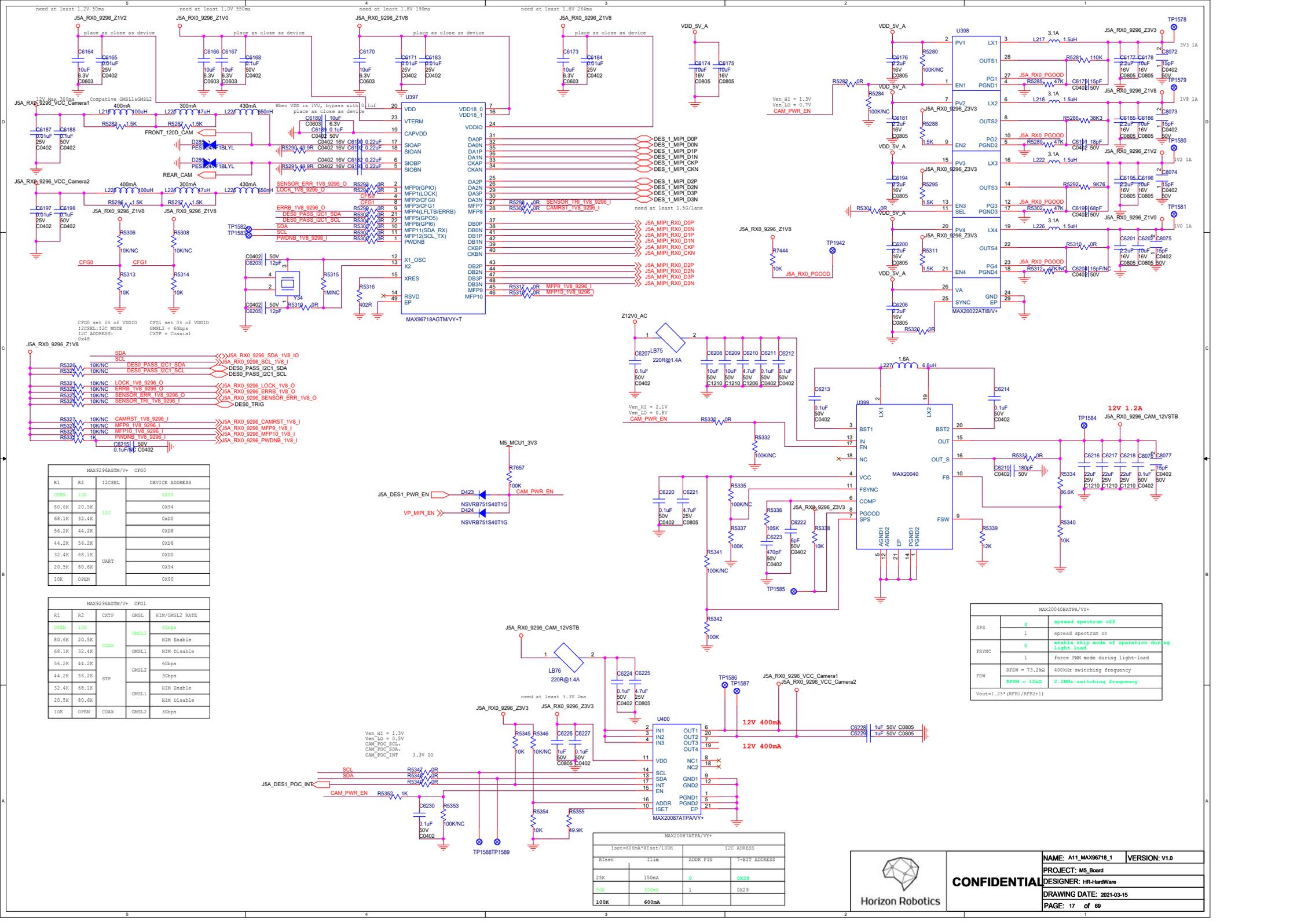
Seq 6

Seq 7



**CONFIDENTIAL**

NAME: 10_Ground	VERSION: v1.0
PROJECT: J5_DVB	
DESIGNER: Horizon Robotics	
DRAWING DATE: 20210128	
PAGE: 16 of 69	



MAX9296AGTM/V+ CFG0

R1	R2	I2CSEL	DEVICE ADDRESS
OPEN	10K		0x90
80.6K	20.5K	I2C	0x94
68.1K	32.4K		0xD0
56.2K	44.2K		0xD8
44.2K	56.2K		0xD8
32.4K	68.1K	I2C	0xD0
20.5K	80.6K		0x94
10K	OPEN		0x90

MAX9296AGTM/V+ CFG1

R1	R2	CXTP	GMSL	HIM/GMSL2 RATE
OPEN	10K		GMSL2	60Gps
80.6K	20.5K		HIM Enable	
68.1K	32.4K	COAX	GMSL1	HIM Disable
56.2K	44.2K		GMSL2	60Gps
44.2K	56.2K	STP	GMSL2	30Gps
32.4K	68.1K		GMSL1	HIM Enable
20.5K	80.6K		GMSL1	HIM Disable
10K	OPEN	COAX	GMSL2	30Gps

MAX20087ATPA/V+

Reset	I11m	ADDR PIN	7-BIT ADDRESS
25K	150mA	0	0x28
50K	300mA	1	0x29
100K	600mA		

MAX20040BATPA/V+

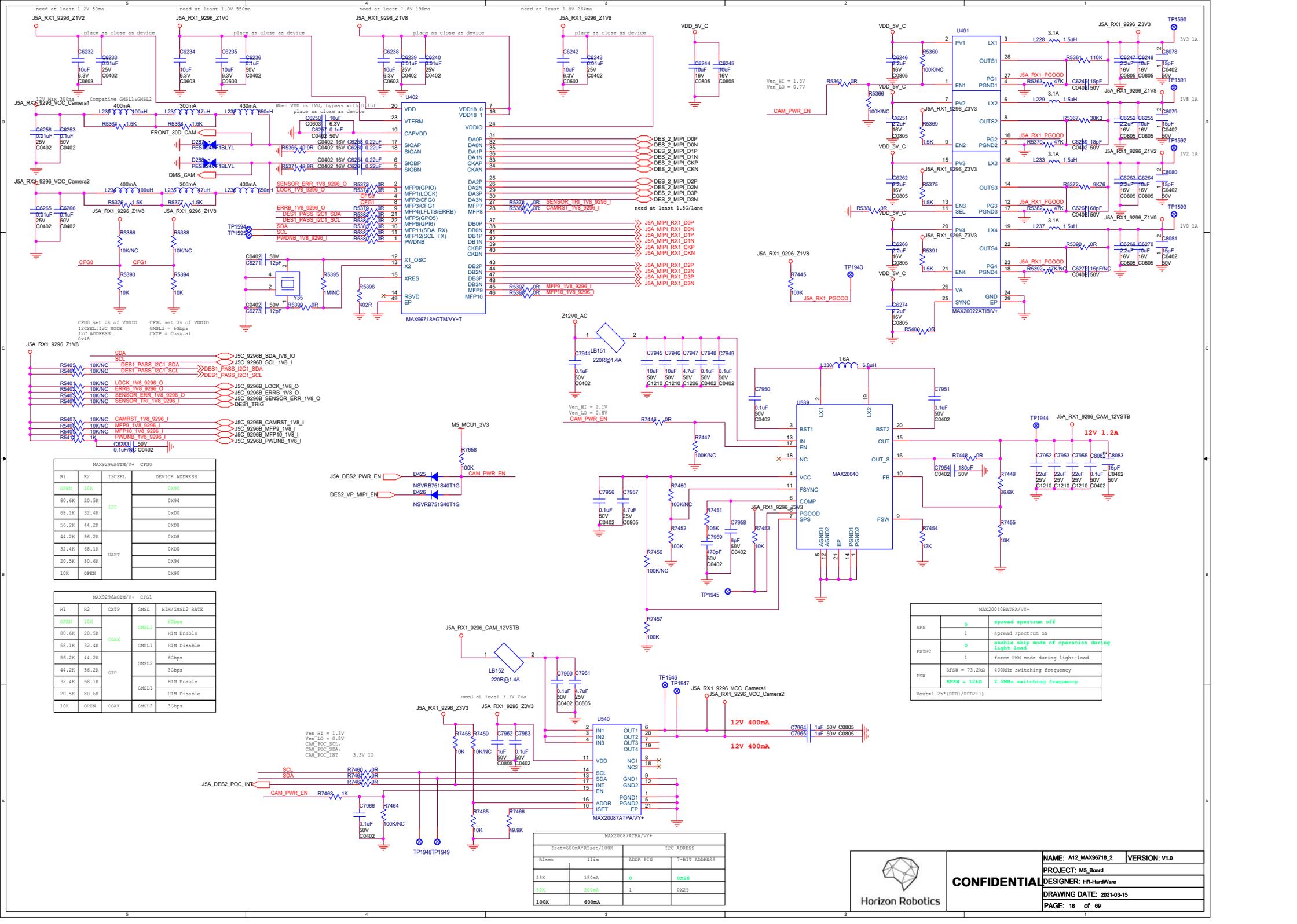
SPS	0	spread spectrum off
SPS	1	spread spectrum on
FSYNC	0	unable skip mode of operation during light load
FSYNC	1	force PWM mode during light-load
FSW	RFSW = 73.2kHz	400kHz switching frequency
	RFSW = 12kHz	2.2MHz switching frequency

Vout=1.25\*(RFB1/RFB2+1)



CONFIDENTIAL

NAME: A11_MAX96718_1	VERSION: v1.0
PROJECT: M5_Board	
DESIGNER: HR-HardWare	
DRAWING DATE: 2021-03-15	
PAGE: 17	of 69



R1	R2	I2CSBL	DEVICE ADDRESS
OPEN	10K		0x50
80.6K	20.5K	I2C	0x94
68.1K	32.4K		0xD0
56.2K	44.2K		0X08
44.2K	56.2K		0X08
32.4K	68.1K	UART	0XD0
20.5K	80.6K		0X94
10K	OPEN		0X30

R1	R2	CXTP	GMSL	HIM/GMSL2 RATE
OPEN	10K		GMSL2	6Gbps
80.6K	20.5K		GMSL1	HIM Enable
68.1K	32.4K	COAX	GMSL1	HIM Disable
56.2K	44.2K		GMSL2	6Gbps
44.2K	56.2K	STP	GMSL1	3Gbps
32.4K	68.1K		GMSL1	HIM Enable
20.5K	80.6K		GMSL1	HIM Disable
10K	OPEN	COAX	GMSL2	3Gbps

SPS	spread spectrum off
0	spread spectrum off
1	spread spectrum on
0	enable skip mode of operation during light load
1	force PWM mode during light-load
FSW	RFSW = 73.2kHz 400kHz switching frequency
	RFSW = 12kHz 2.0MHz switching frequency

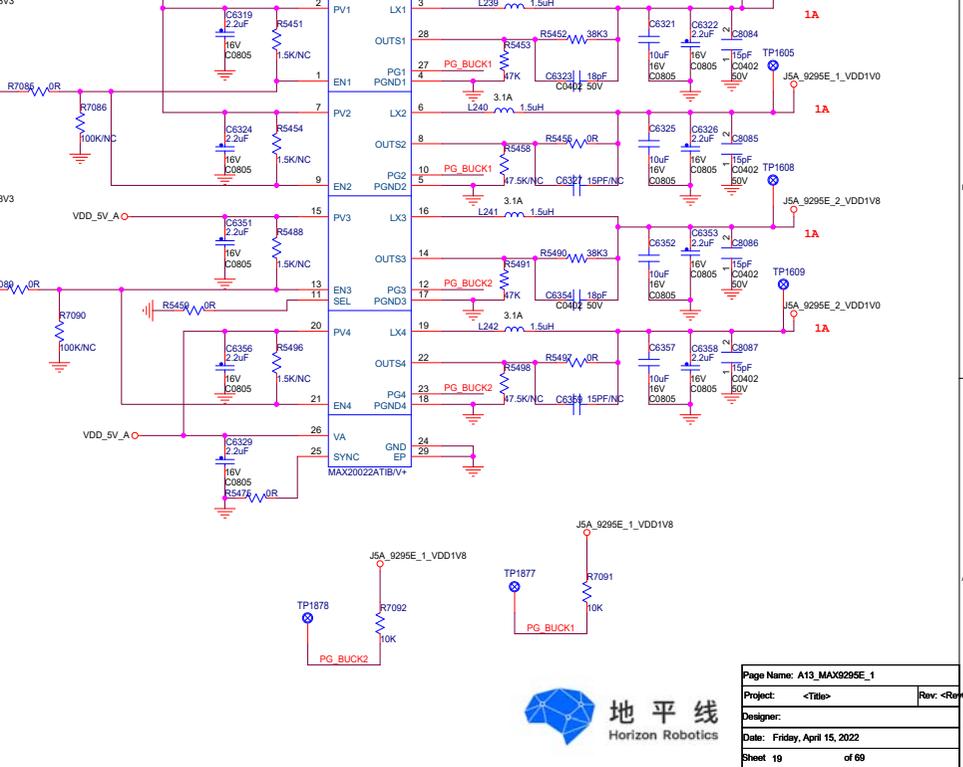
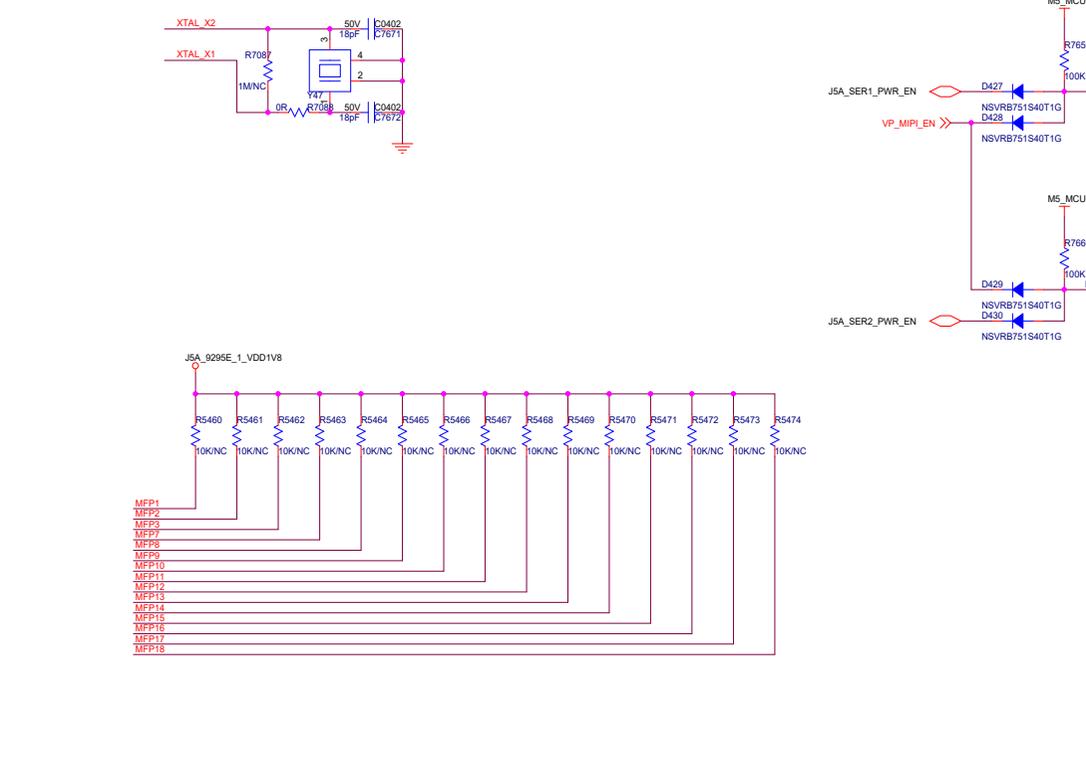
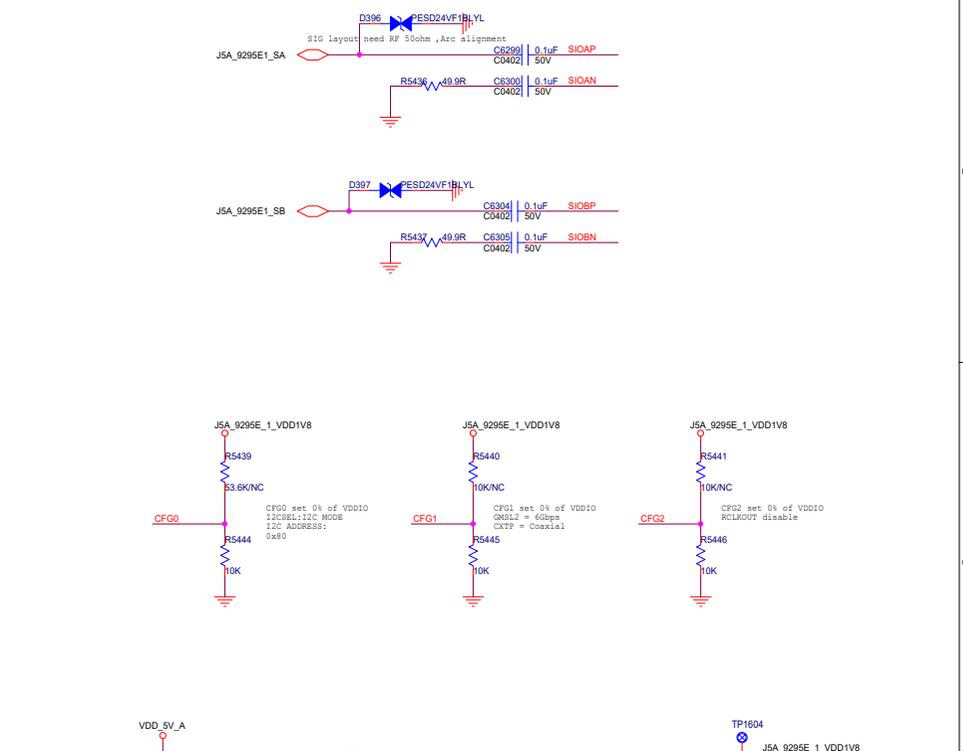
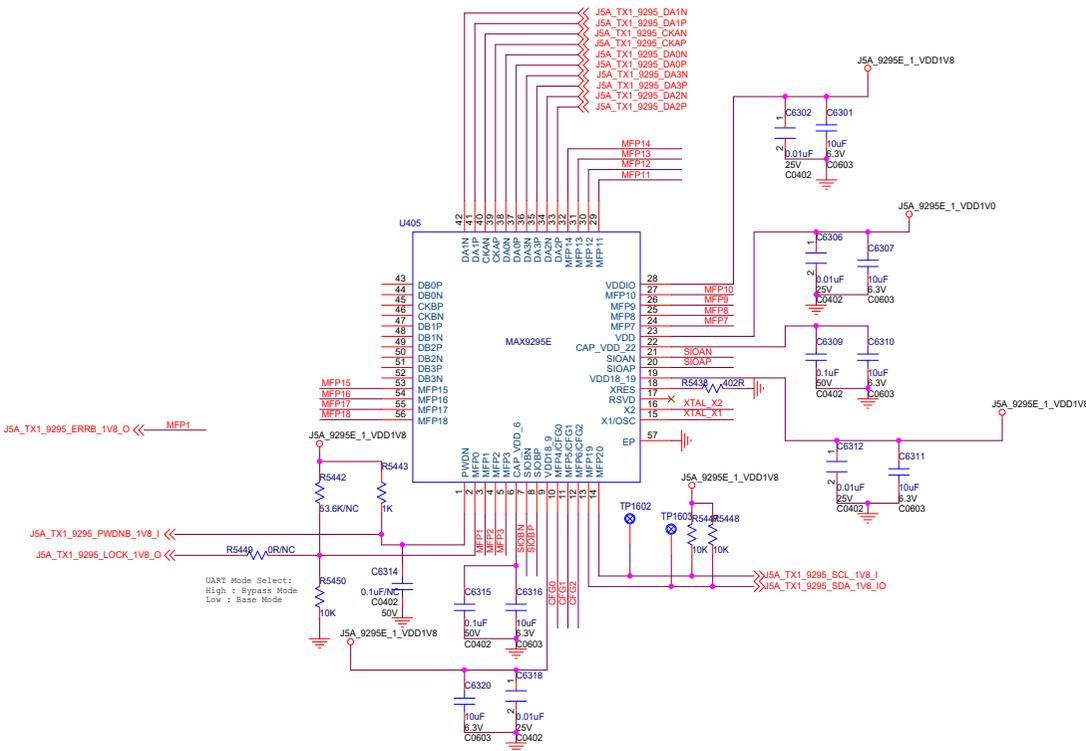
Wout=1.25\*(RFS1/RFS2+1)

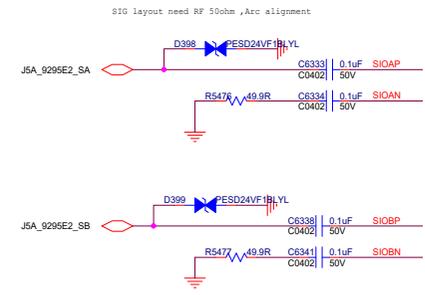
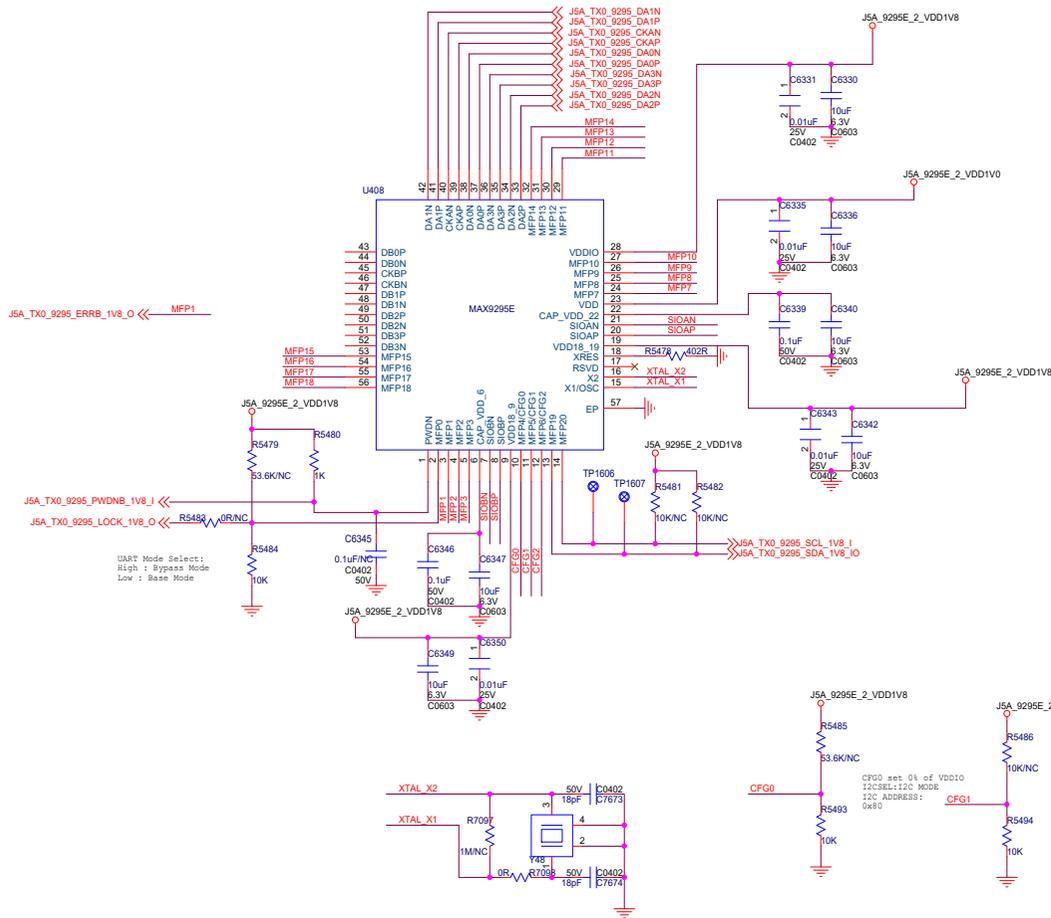
Iset#00mA*Reset/100k	I2C ADDRESS
Reset	111m ADDR PIN 7-BIT ADDRESS
25K	150mA 0 0x28
50K	300mA 1 0x29
100K	600mA



**CONFIDENTIAL**

NAME: A12\_MAX96718\_2 | VERSION: v1.0  
 PROJECT: M5\_Board  
 DESIGNER: HR-HardWare  
 DRAWING DATE: 2021-03-15  
 PAGE: 18 of 89





JSA\_TX0\_9295\_ERRB\_1V8\_O << MFP1

JSA\_TX0\_9295\_PWDNB\_1V8\_I <<

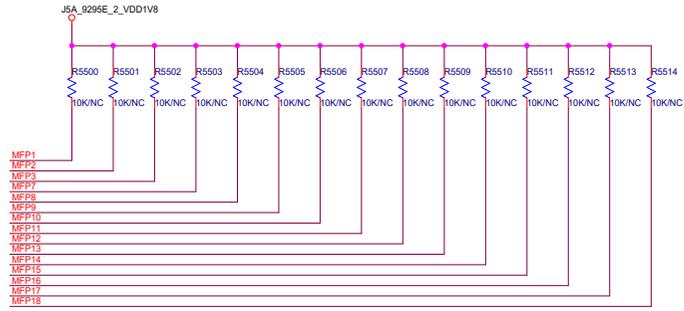
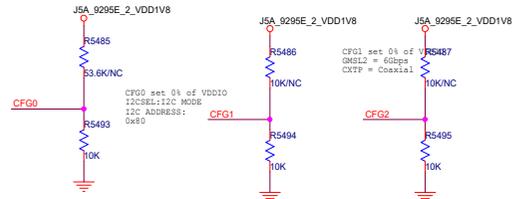
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JSA\_9295E\_2\_VDD1V8

JSA\_9295E\_2\_VDD1V0

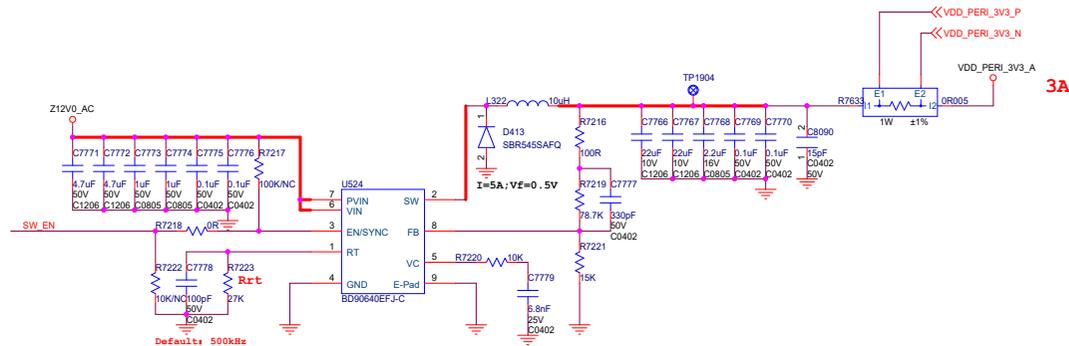
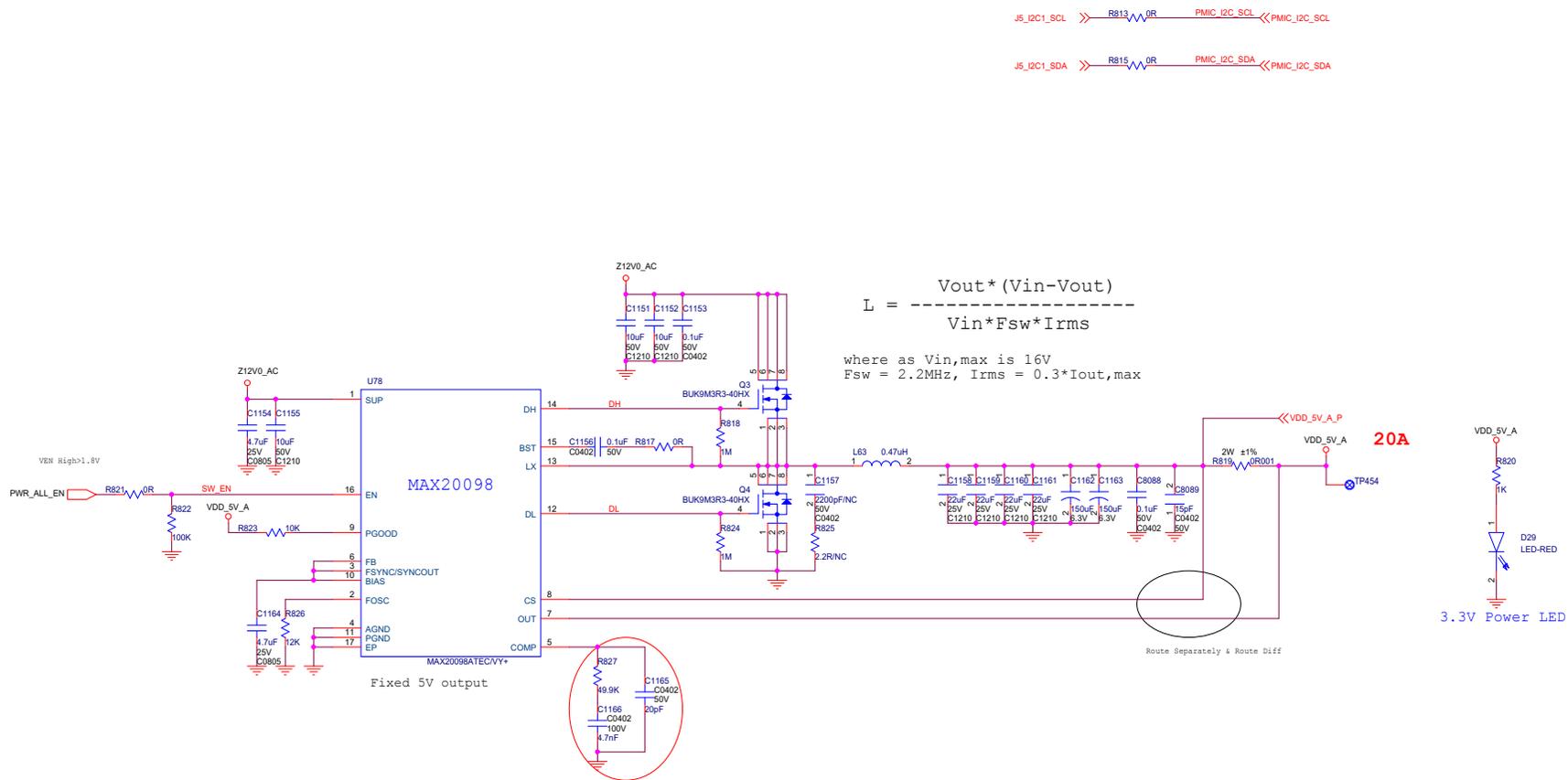
JSA\_9295E\_2\_VDD1V8

UART Mode Select  
High : Bypass Mode  
Low : Base Mode



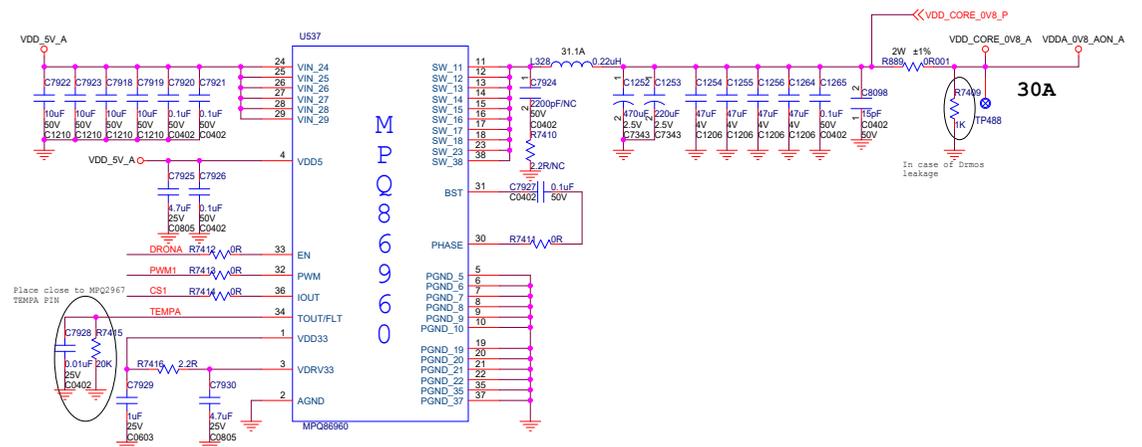
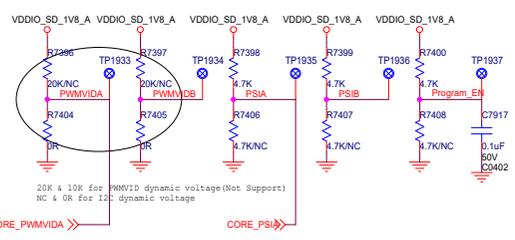
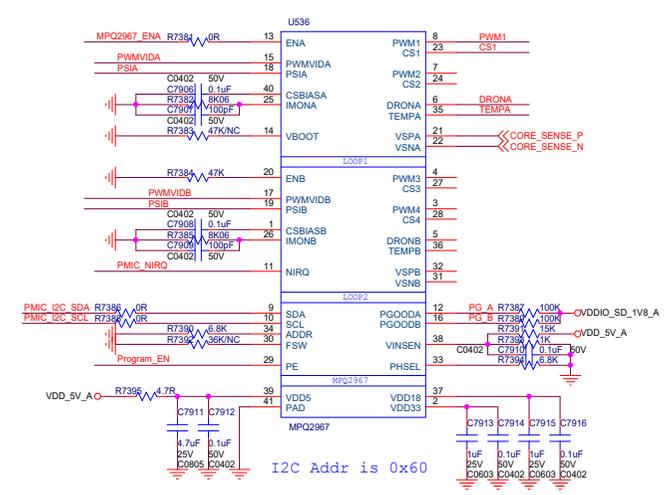
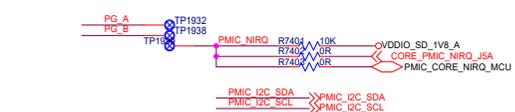
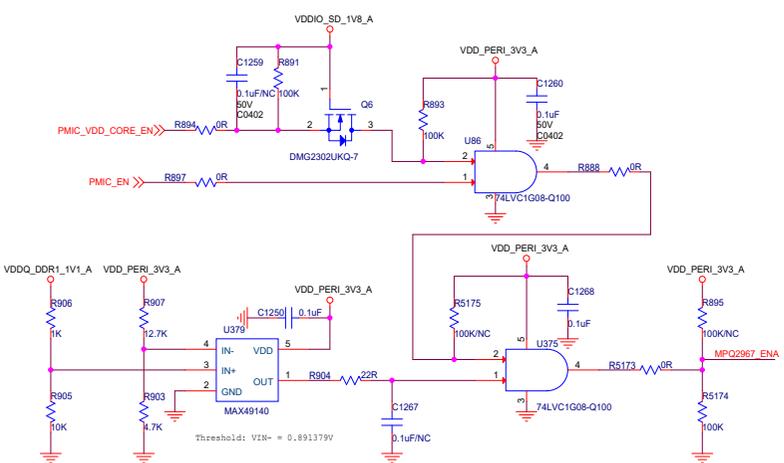
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Designer:		
Date: Saturday, April 02, 2022		
Sheet: 20 of 68		











**CONFIDENTIAL**

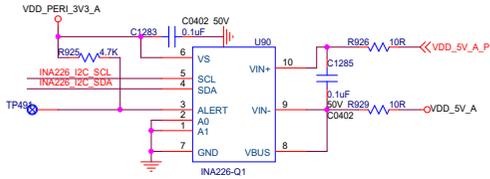
NAME: 05_PFK200MLDO	VERSION: v1.0
PROJECT: J5_DVB	
DESIGNER: Horizon Robotics	
DRAWING DATE: 20210128	
PAGE: 25 of 69	

INA226 settings:  
 Shunt Voltage Register LSB : 2.5uV/bit  
 Bus Voltage Register LSB : 1.25mV/bit  
 Power Register LSB : 25\*Current\_LSB

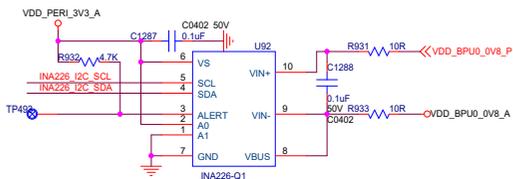
Current\_LSB = {Maximum Expected Current}/2^15  
 CAL = 0.00512/(Current\_LSB \* Rshunt)  
 Current\_Register(04H) = {Shunt Voltage Register}\*(CAL)/2048  
 Power = {Bus Voltage Register(02H)}\*(Current\_Register(04H))/20000

(1) For Current rating up to 10A~20A level  
 Current\_LSB =  $\frac{10.000\text{ mA}}{2^{15}}$  = 305.1757812 uA/bit  
 Set Current\_LSB as 1mA/bit  
 Rshunt = 0.001 Ohm , So  
 CAL =  $\frac{0.00512}{1\text{ mA/bit} \times 0.001\text{ Ohm}}$  = 5120

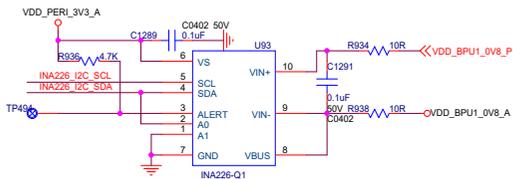
(2) For Current rating up to <= 3A level  
 Current\_LSB =  $\frac{3.000\text{ mA}}{2^{15}}$  = 91.55273438 uA/bit  
 Set Current\_LSB as 200uA/bit  
 Rshunt = 0.005 Ohm , So  
 CAL =  $\frac{0.00512}{200\text{ uA/bit} \times 0.005\text{ Ohm}}$  = 5120



I2C Address: 100-0000 (0x40)

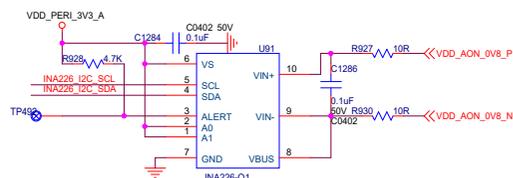


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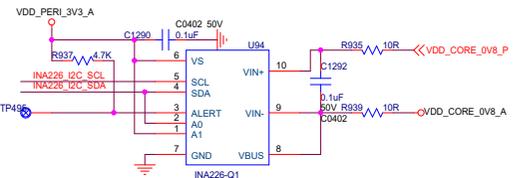


I2C Address: 100-0010 (0x42)

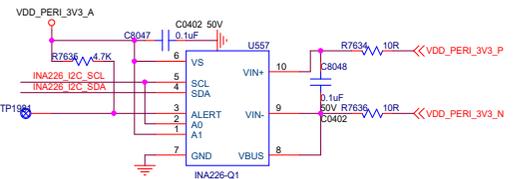
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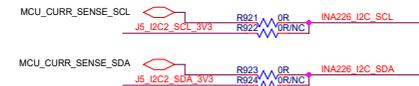
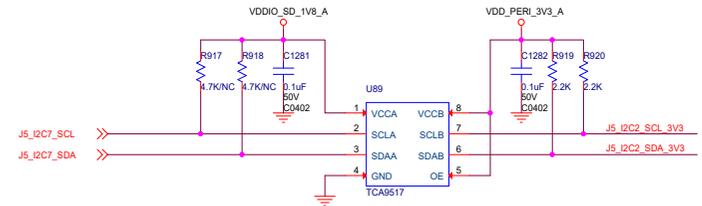
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I2C Address: 100-0110 (0x46)

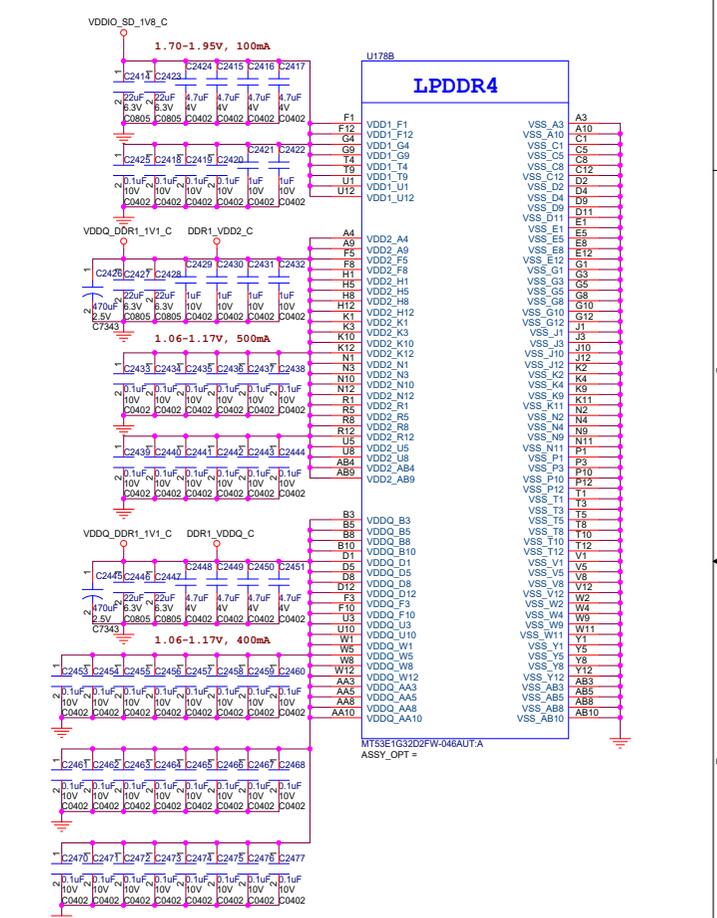
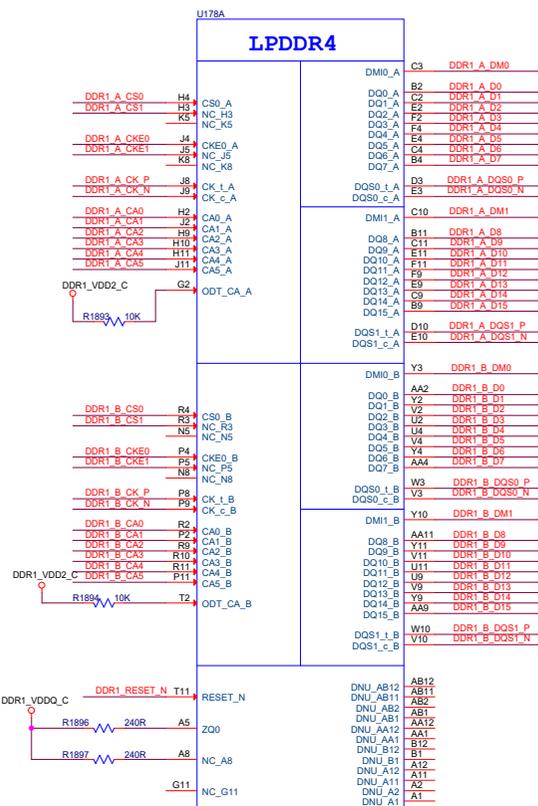
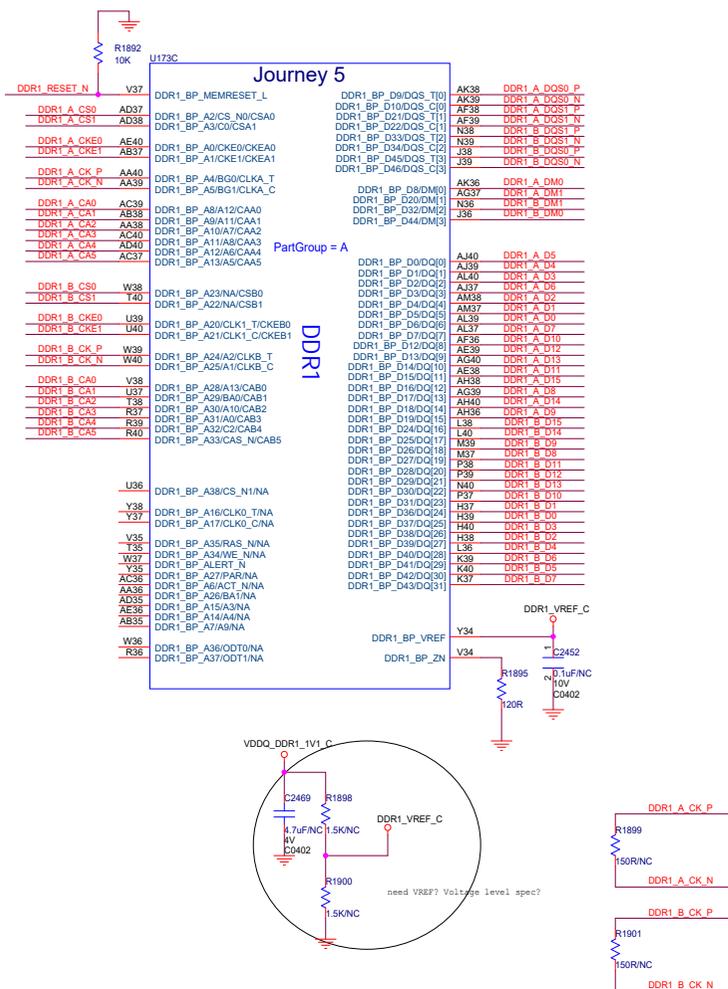


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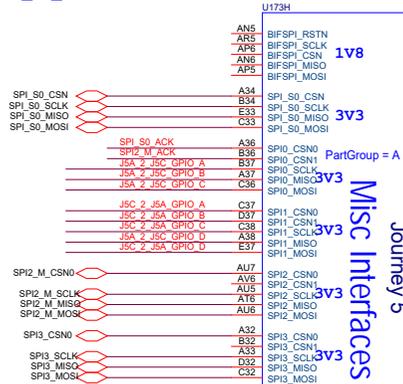
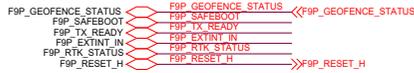


SK DDR Design guide:  
 (1) VDD1 : one de-cap for VDD1/VSS per about two VDD1 balls  
 (2) VDD2 : 100nF\*3+1uF per DRAM die  
 (3) VDDQ : 100nF\*4+4.7uF per DRAM die

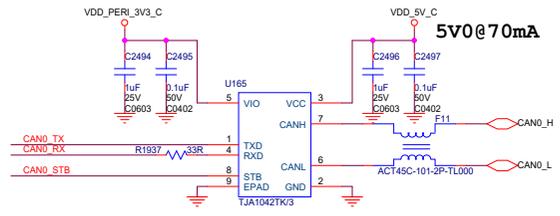
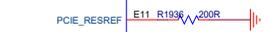
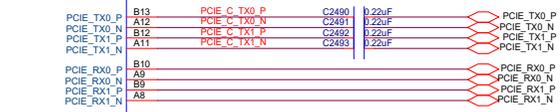
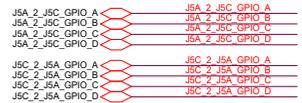
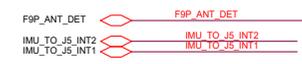
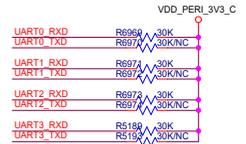
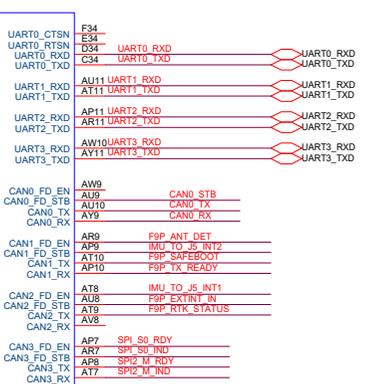


VDDIO\_SD\_SPI2/3/S0/BIFSPI--3V3

VDDIO\_SD\_SPI0/1--1V8



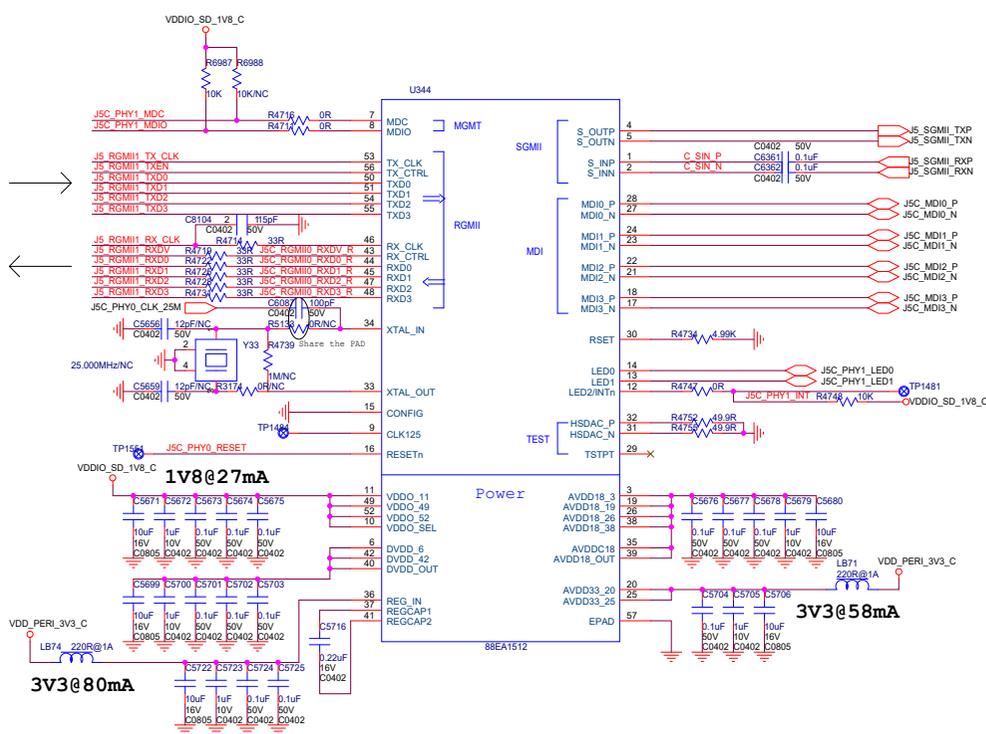
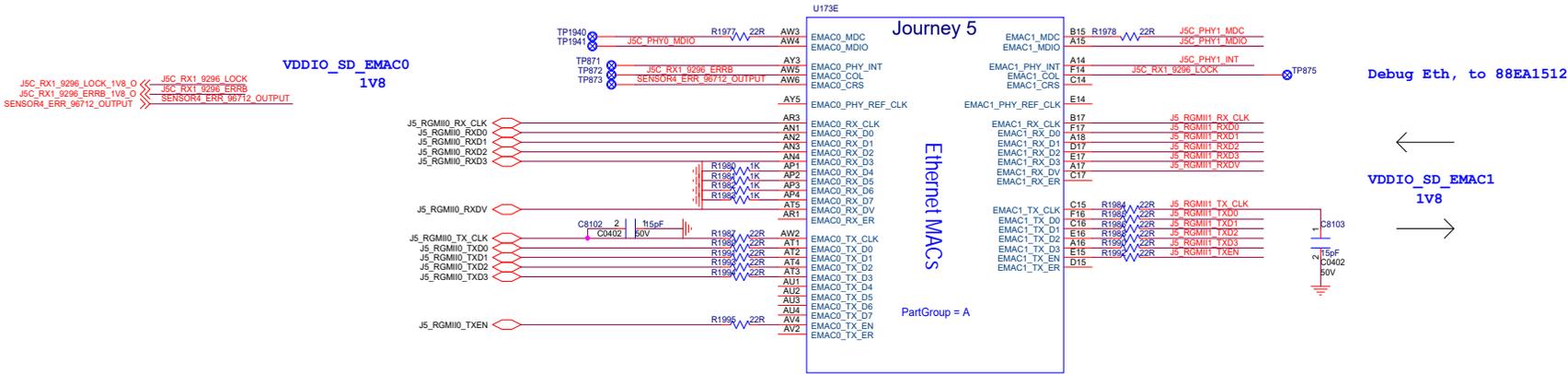
Misc Interfaces  
Journey 5

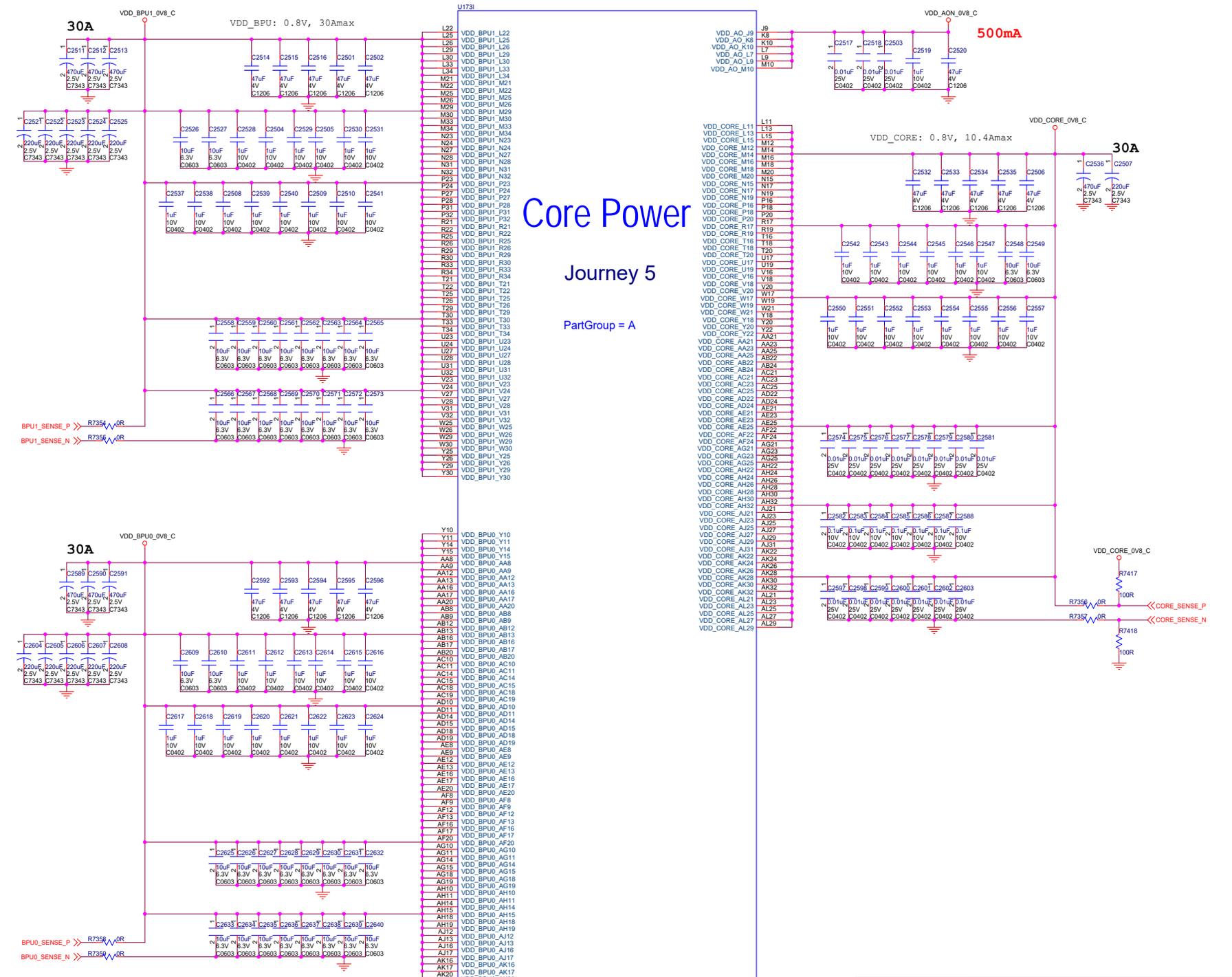


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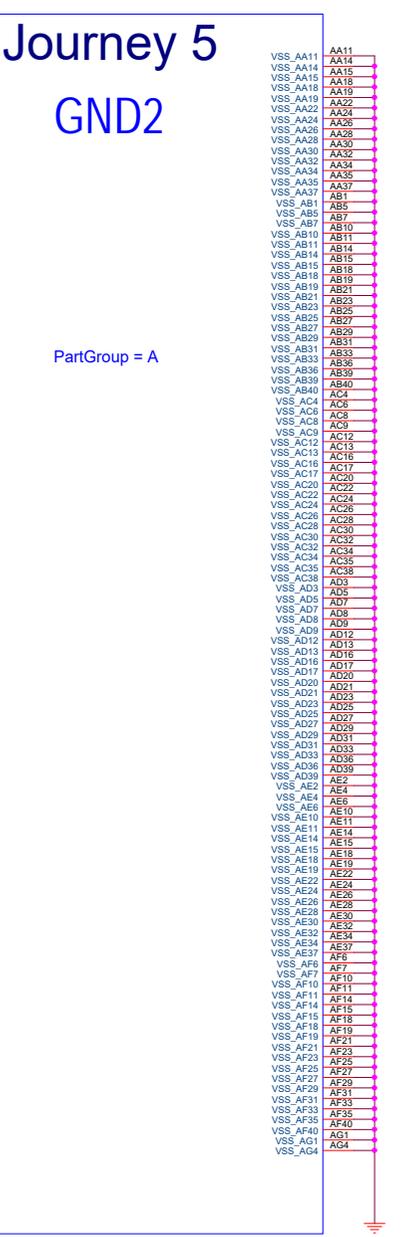
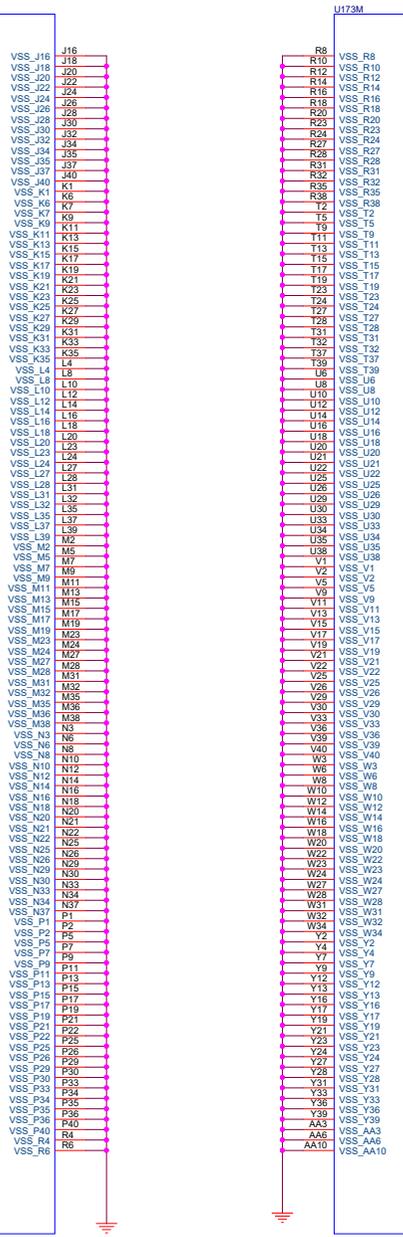
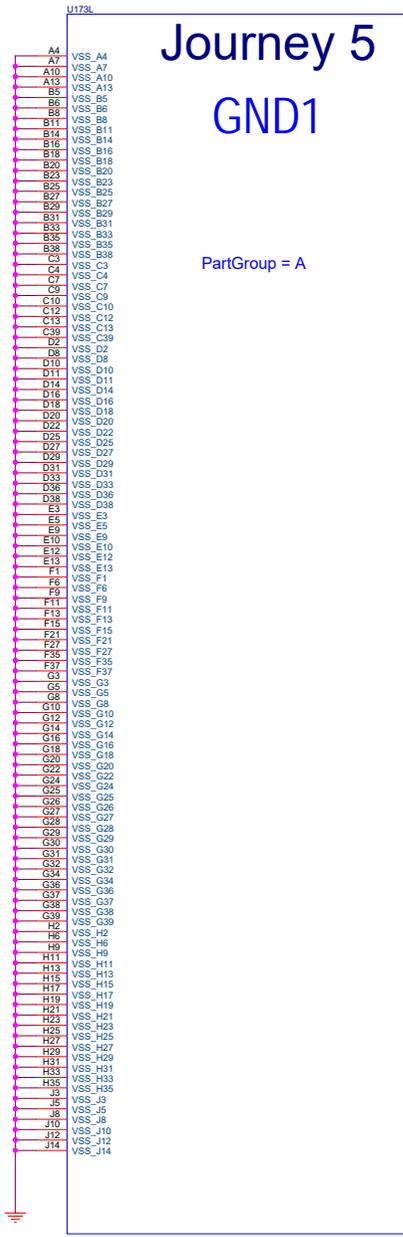
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PROJECT: J5_DVB	
DESIGNER: Horizon Robotics	
DRAWING DATE: 20210128	
PAGE: 31 of 69	





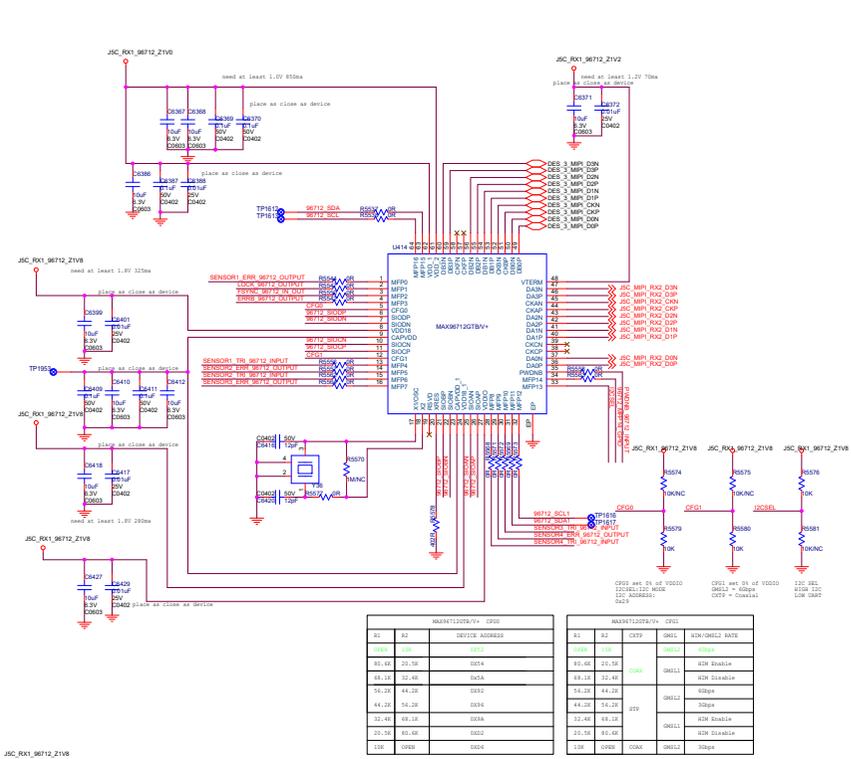




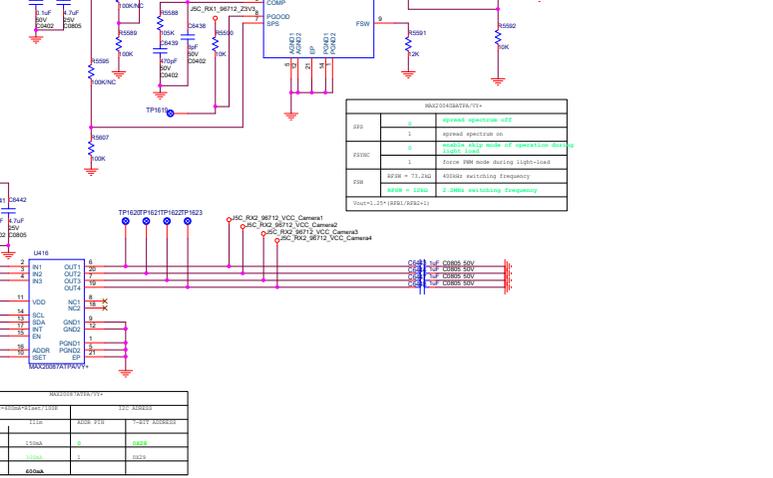
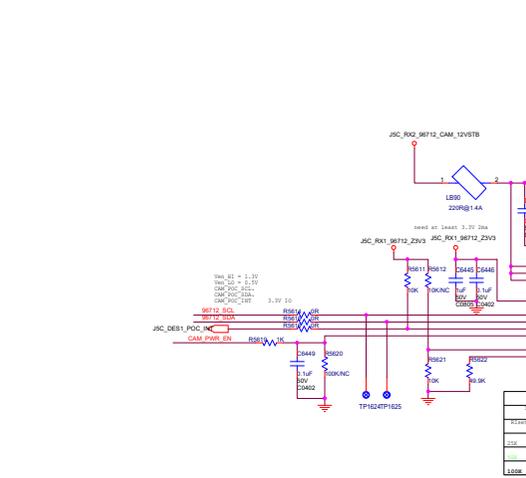
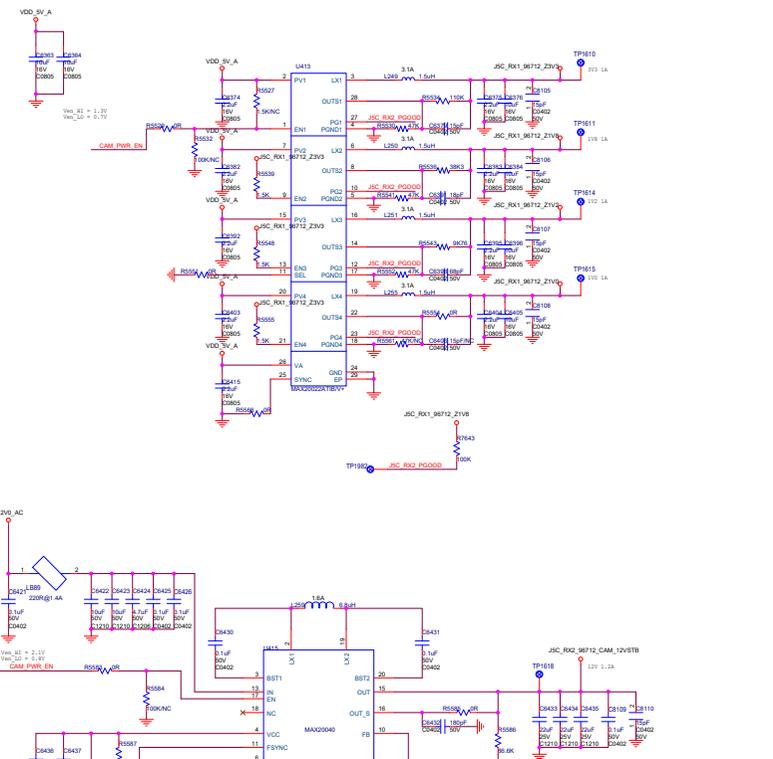
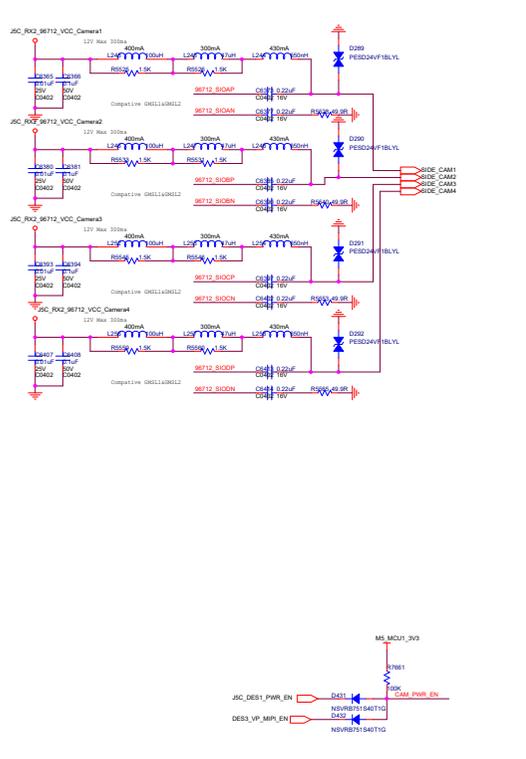
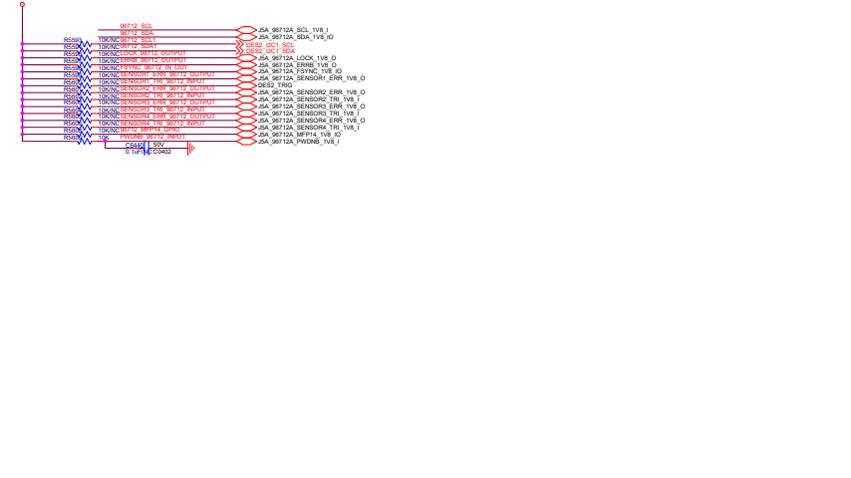


**CONFIDENTIAL**

NAME: 10_Ground	VERSION: v1.0
PROJECT: J5_DWB	
DESIGNER: Horizon Robotics	
DRAWING DATE: 20210128	
PAGE: 36 of 69	



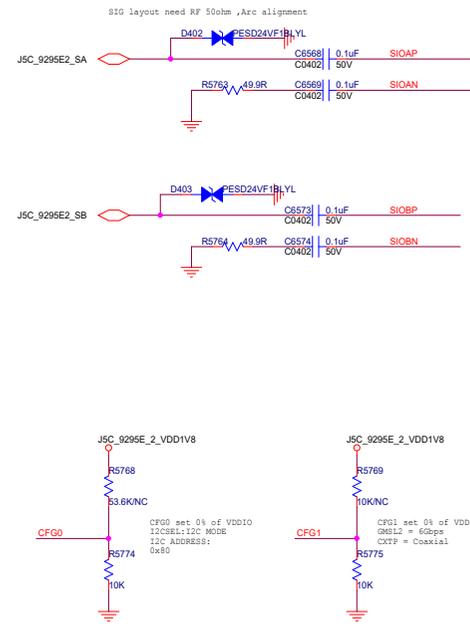
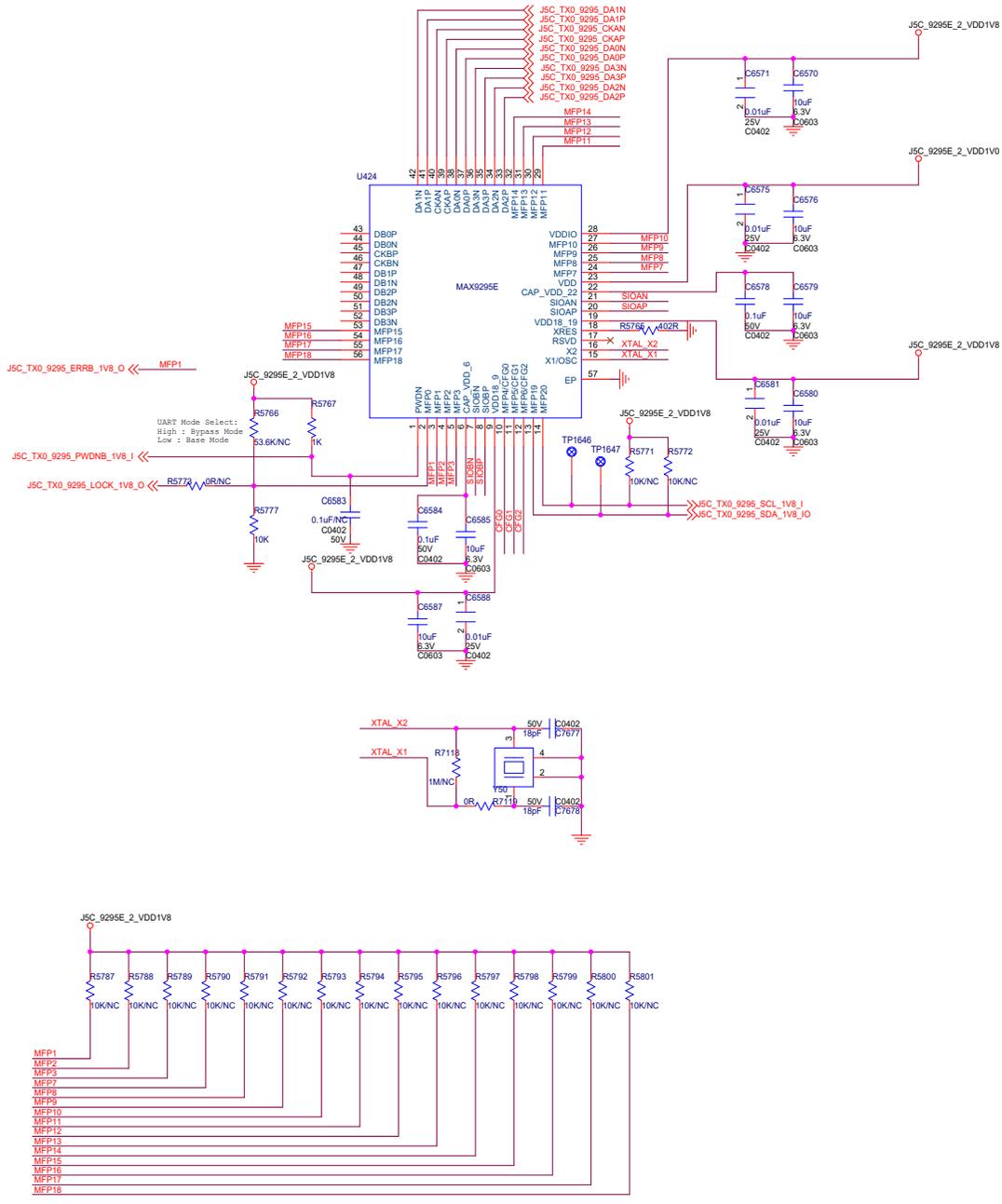
MA9812028V_V1 - CS10				MA9812028V_V1 - CS10			
R1	R2	DEVICE ADDRESS	CS10	R1	R2	CS10	MEM/DRIVE RATE
0x00	1.00	0x00	0x00	0x00	1.00	0x00	0x00
0x.00	20.00	0x04	0x04	0x.00	20.00	0x04	0x04
0x.10	32.00	0x08	0x08	0x.10	32.00	0x08	0x08
0x.20	44.00	0x0C	0x0C	0x.20	44.00	0x0C	0x0C
0x.30	56.00	0x10	0x10	0x.30	56.00	0x10	0x10
0x.40	68.00	0x14	0x14	0x.40	68.00	0x14	0x14
0x.50	80.00	0x18	0x18	0x.50	80.00	0x18	0x18
0x.60	92.00	0x1C	0x1C	0x.60	92.00	0x1C	0x1C
0x.70	104.00	0x20	0x20	0x.70	104.00	0x20	0x20
0x.80	116.00	0x24	0x24	0x.80	116.00	0x24	0x24
0x.90	128.00	0x28	0x28	0x.90	128.00	0x28	0x28



MA9812028V_V1 - CS10			
R1	R2	DEVICE ADDRESS	CS10
0x00	1.00	0x00	0x00
0x.00	20.00	0x04	0x04
0x.10	32.00	0x08	0x08
0x.20	44.00	0x0C	0x0C
0x.30	56.00	0x10	0x10
0x.40	68.00	0x14	0x14
0x.50	80.00	0x18	0x18
0x.60	92.00	0x1C	0x1C
0x.70	104.00	0x20	0x20
0x.80	116.00	0x24	0x24
0x.90	128.00	0x28	0x28





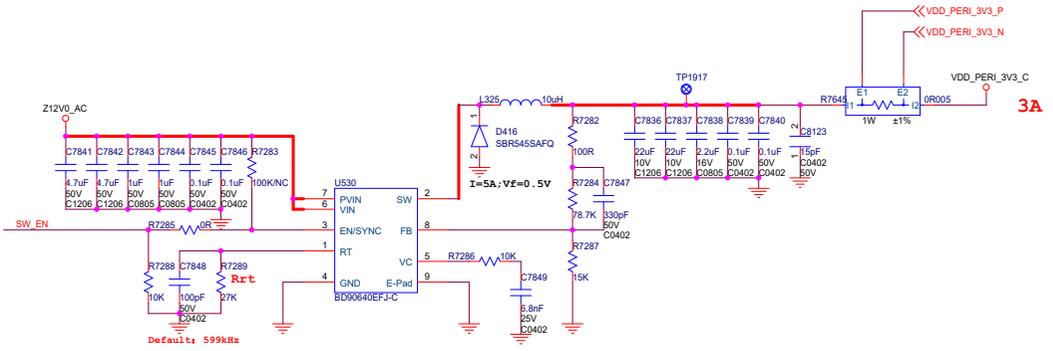
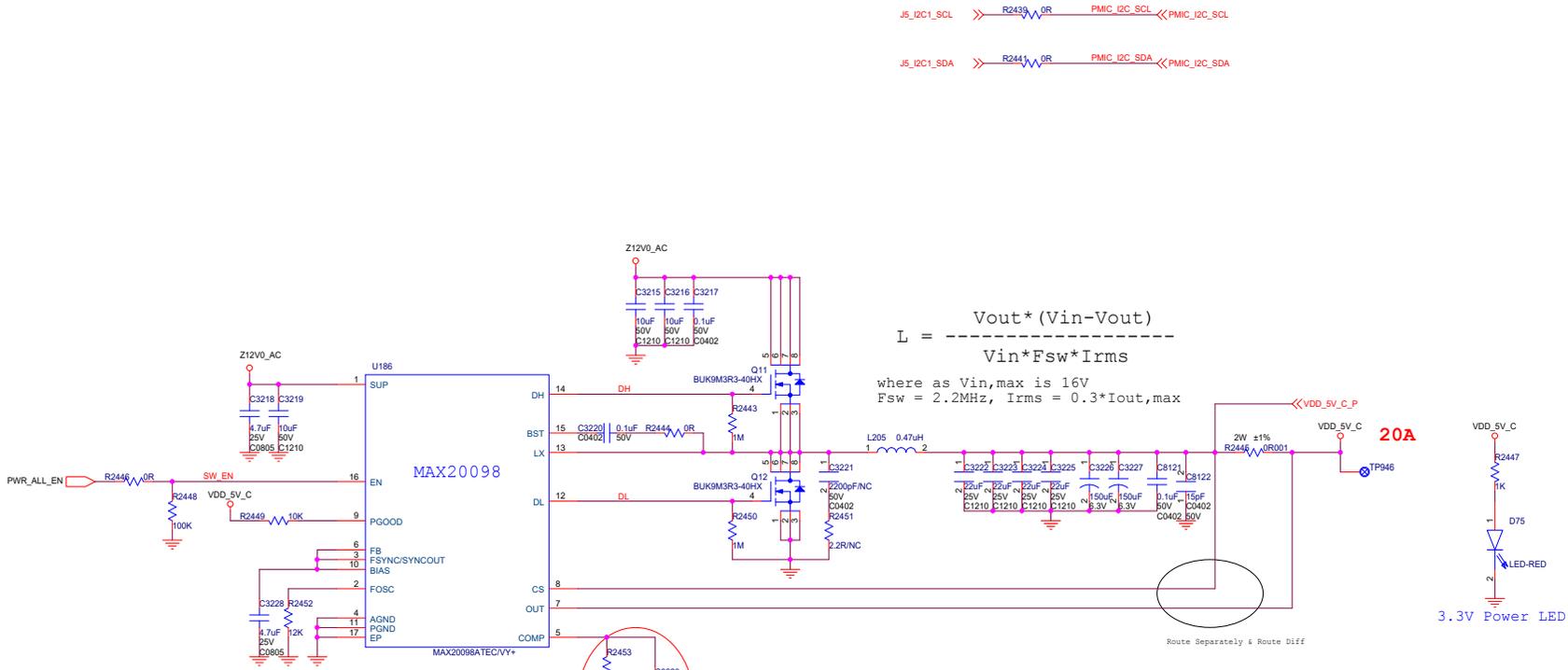




Horizon Robotics

**CONFIDENTIAL**

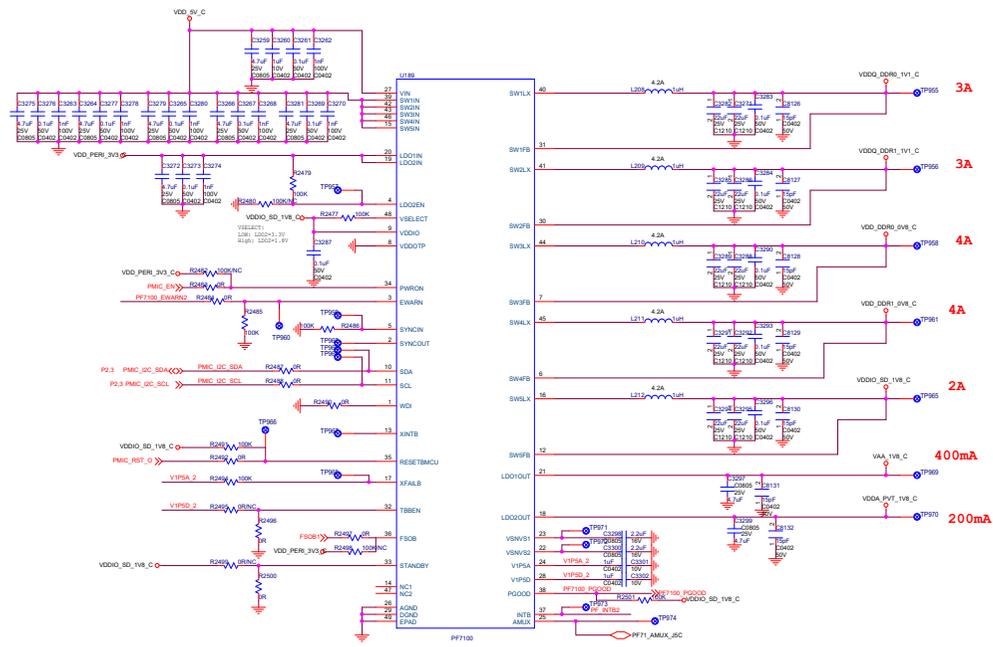
NAME: 01_Powertrain	VERSION: V1.0
PROJECT: JS_DW8	
DESIGNER: Horizon Robotics	
DRAWING DATE: 20210128	
PAGE: 41	of 69



**CONFIDENTIAL**

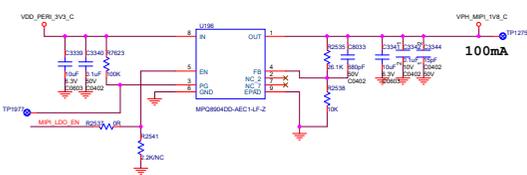
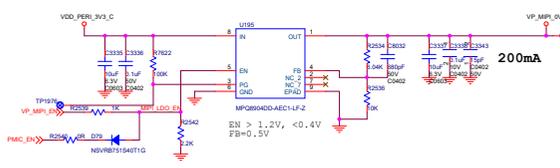
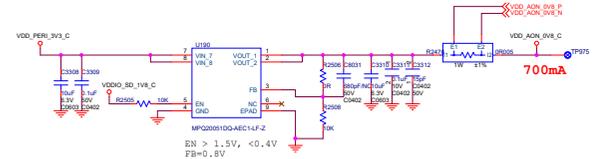
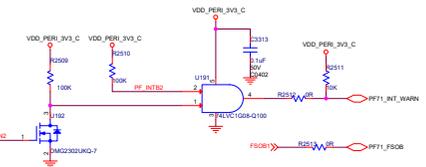
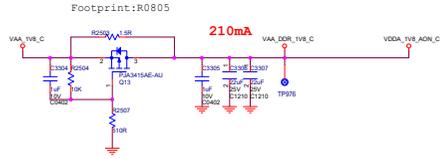
NAME: 02_z5v0	VERSION: v1.0
PROJECT: J5_DVB	
DESIGNER: Horizon Robotics	
DRAWING DATE: 20210128	
PAGE: 42 of 69	





PF7100 I2C Address is set by the OTP\_I2C\_ADD[2:0], range from 0x08-0x0F

- (1) DO NOT supply VQPS EFUSE before PF7100\_PG is High.
- (2) Short TP1956 and TP1957 to supply VQPS\_EFUSE.





INA226 settings:  
 Shunt Voltage Register LSB : 2.5uV/bit  
 Bus Voltage Register LSB : 1.25mV/bit  
 Power Register LSB : 25\*Current\_LSB

Current\_LSB = {Maximum Expected Current}/2^15  
 CAL = 0.00512/(Current\_LSB \* Rshunt)  
 Current\_Register(04H) = {Shunt Voltage Register}\*(CAL)/2048  
 Power = {Bus Voltage Register(02H)}\*(Current\_Register(04H))/20000

(1) For Current rating up to 10A~20A level

$$\text{Current\_LSB} = \frac{10.000 \text{ mA}}{2^{15}} = 305.1757812 \text{ uA/bit}$$

Set Current\_LSB as 1mA/bit

Rshunt = 0.001 Ohm , So

$$\text{CAL} = \frac{0.00512}{1 \text{ mA/bit} \times 0.001 \text{ Ohm}} = 5120$$

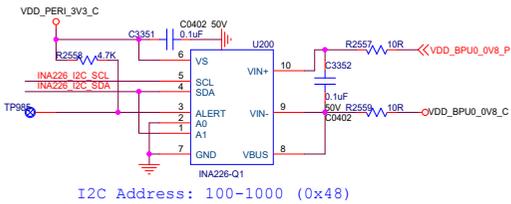
(2) For Current rating up to <= 3A level

$$\text{Current\_LSB} = \frac{3.000 \text{ mA}}{2^{15}} = 91.55273438 \text{ uA/bit}$$

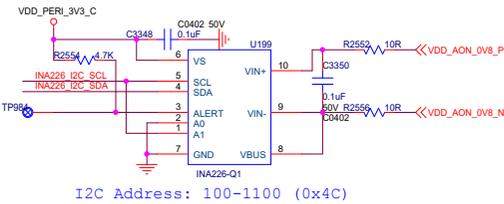
Set Current\_LSB as 200uA/bit

Rshunt = 0.005 Ohm , So

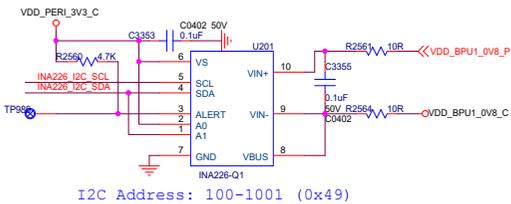
$$\text{CAL} = \frac{0.00512}{200 \text{ uA/bit} \times 0.005 \text{ Ohm}} = 5120$$



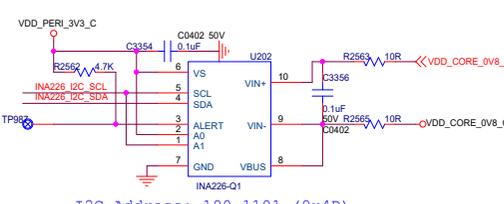
I2C Address: 100-1000 (0x48)



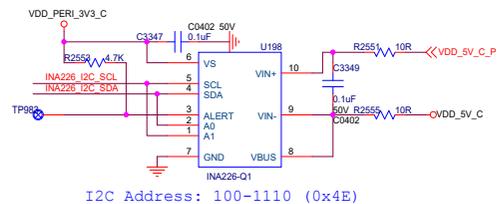
I2C Address: 100-1100 (0x4C)



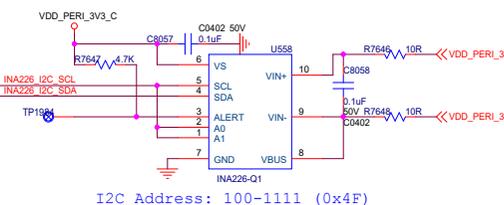
I2C Address: 100-1001 (0x49)



I2C Address: 100-1101 (0x4D)

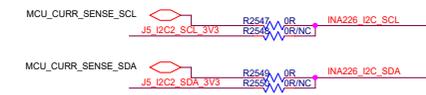
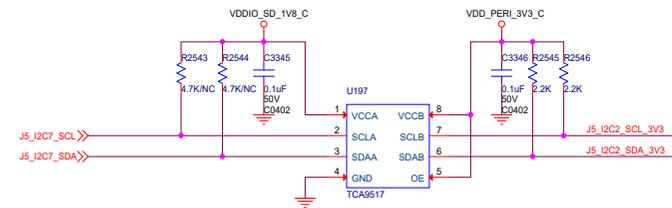


I2C Address: 100-1110 (0x4E)



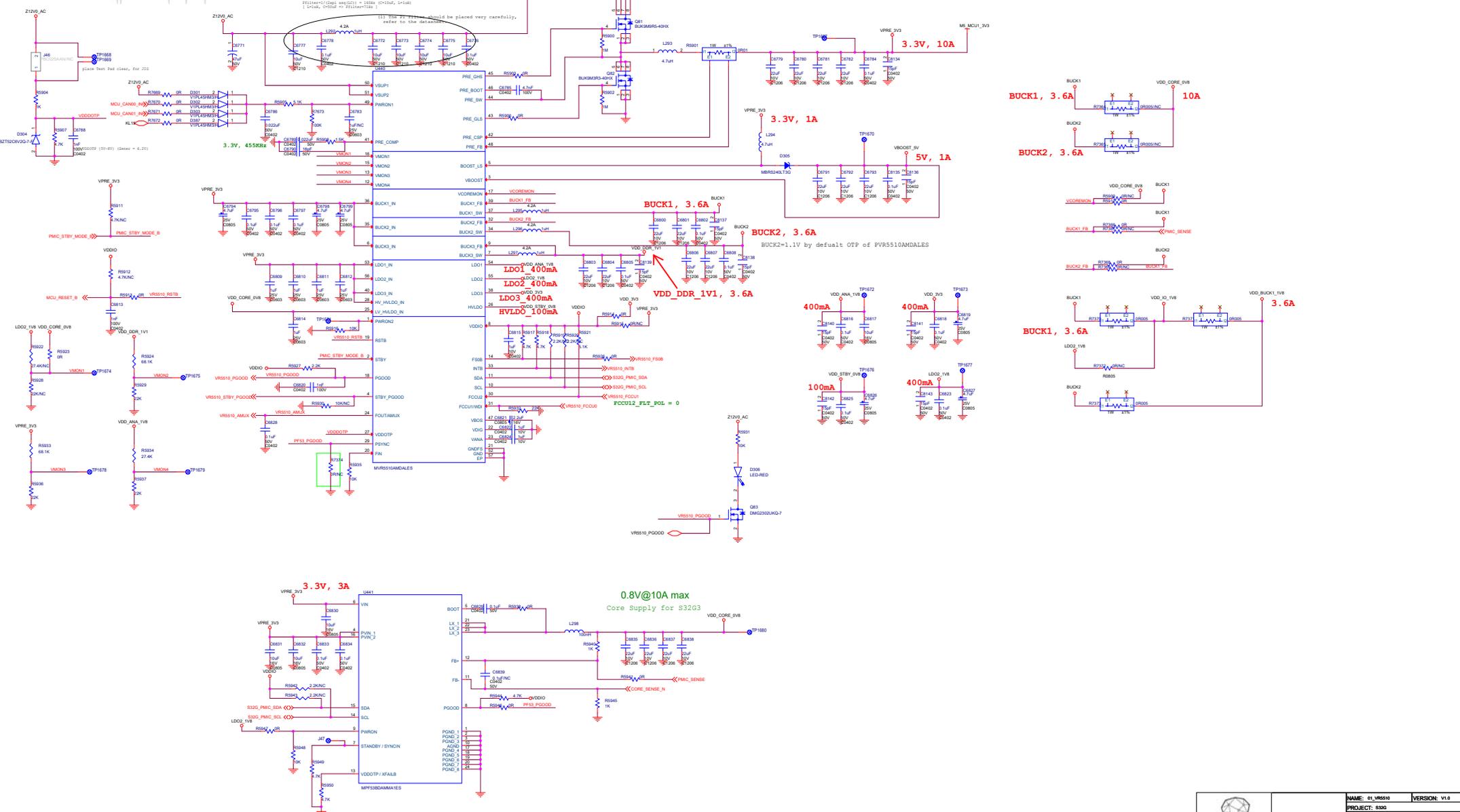
I2C Address: 100-1011 (0x4F)

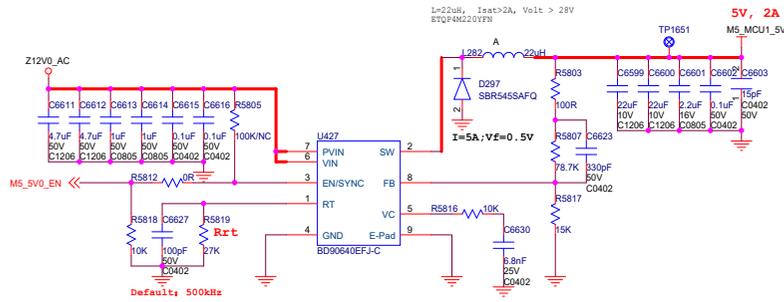
I2C Address: 100-1111 (0x4F)



Rev	Description	Date
1	Initial Release	2021-11-22
2	MCU CAN1, IN0, IN1	2021-11-22
3	MCU CAN1, IN0, IN1	2021-11-22

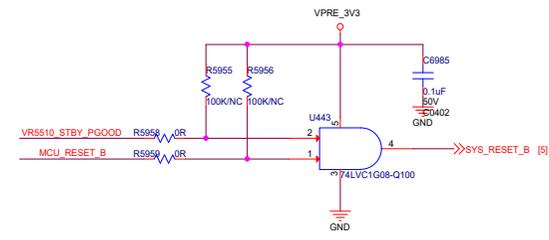
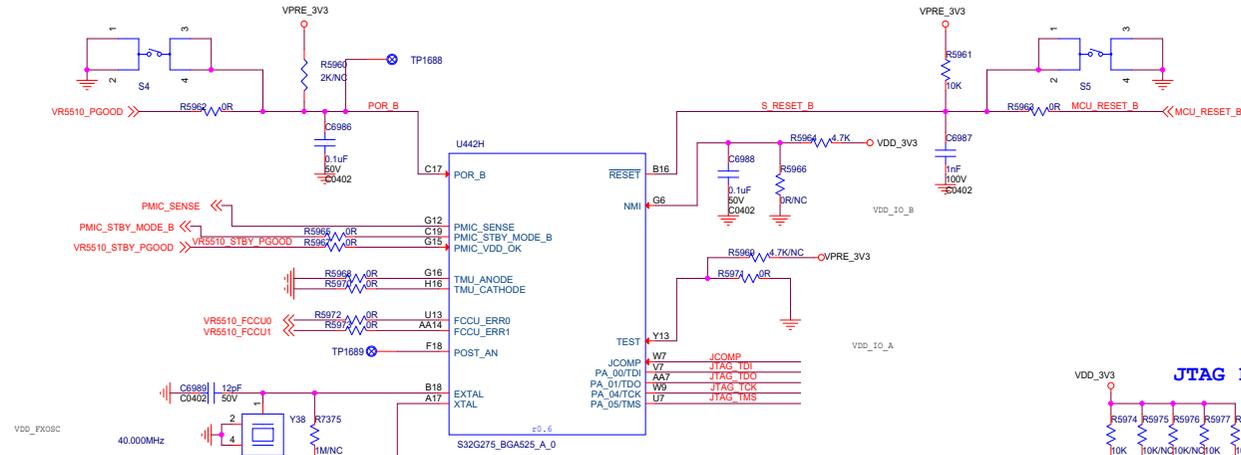
(2) C bootstrap value > 10k Cps\_Q  
 (3) Place resistor between Gate\_Source of Q



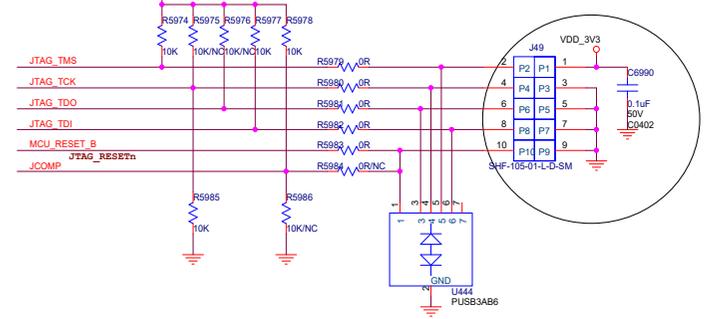




# MCU RESET CIRCUIT



# JTAG For DS-5



U442D

AUR_CLK_P	AC11	TP1853
AUR_CLK_N	AB11	TP1854
AUR_TX0_P	AC8	TP1855
AUR_TX0_N	AB8	TP1856
AUR_TX1_P	AB6	TP1857
AUR_TX1_N	AC6	TP1858
AUR_TX2_P	AC9	TP1859
AUR_TX2_N	AB9	TP1860
AUR_TX3_P	AB5	TP1861
AUR_TX3_N	AC5	TP1862

S32G275\_BGA525\_A\_0

# AURORA



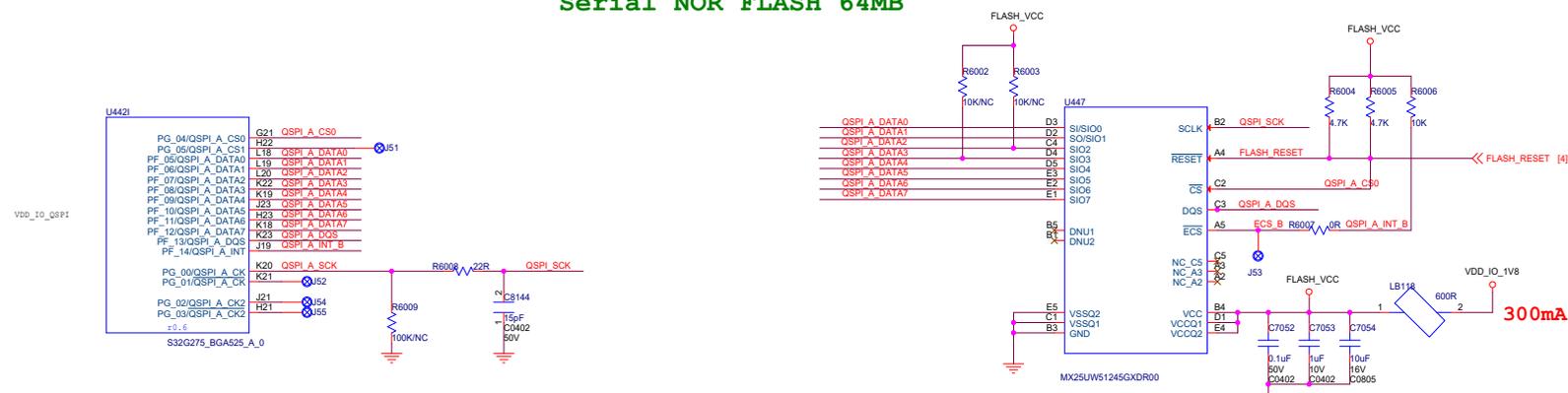
**CONFIDENTIAL**

NAME: 04_RESET_ITAG	VERSION: v1.0
PROJECT: S32G	
DESIGNER: Horizon Robotics	
DRAWING DATE: 20211122	
PAGE: 50	of 69

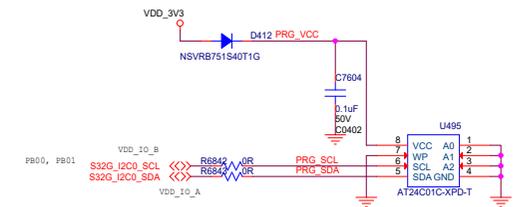
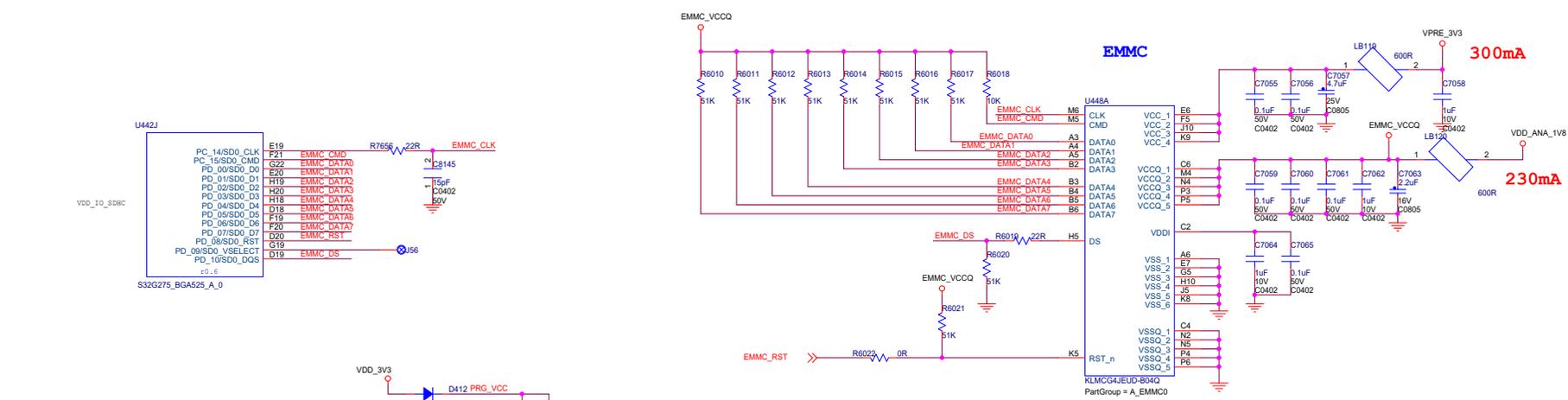


# Serial NOR FLASH 64MB

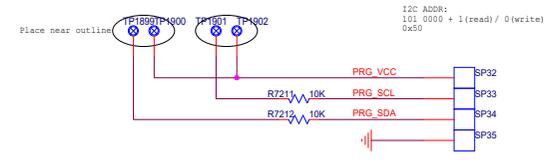
OPEN DRAIN FOR LEVEL SHIFTER



# 32GB eMMC MEMORY 5.1



I2C0 ADDR: 0XA0

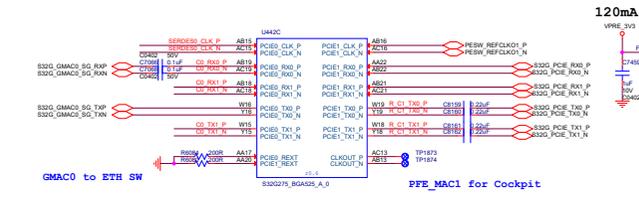


**CONFIDENTIAL**

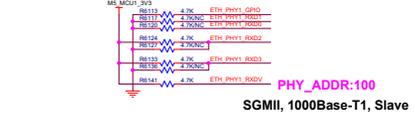
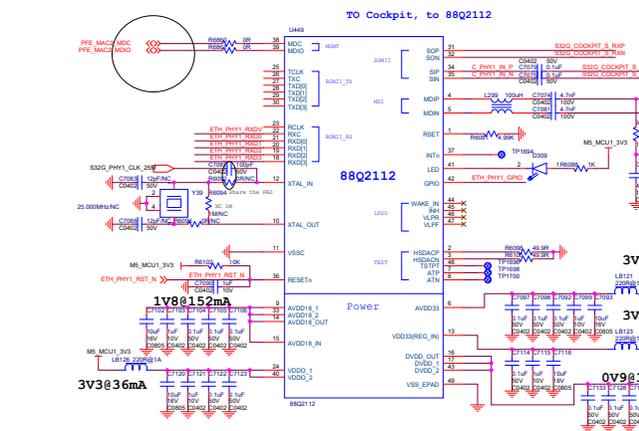
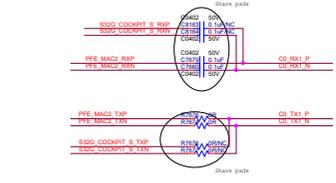
NAME: 05_FLASH_EMMC	VERSION: v1.0
PROJECT: S32G	
DESIGNER: Horizon Robotics	
DRAWING DATE: 20211122	
PAGE: 52 of 69	







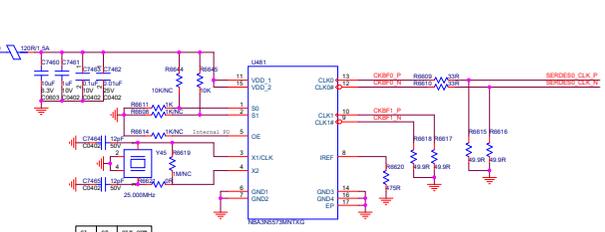
Serdes_0	Lane 0	Lane 1	Serdes_1	Lane 0	Lane 1
Mode 3	SGMI (GMAC 0) to ETH SW For7	SGMI (PFE MAC2) to Cockpit 4Dog R3	Mode 0	PCIe1_x2	PCIe1_x2



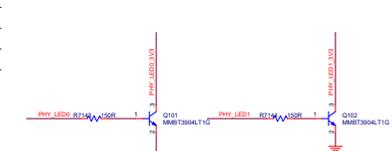
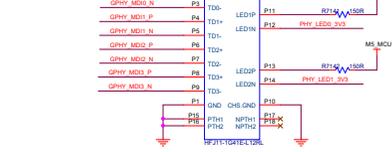
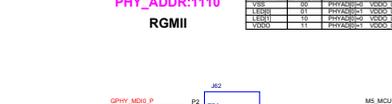
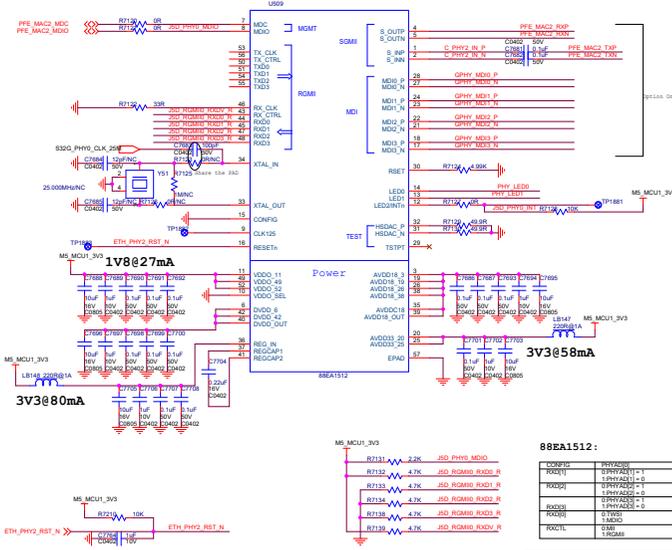
88Q2112:	
CS0	PHY_ADDR0
CS1	PHY_ADDR1
CS2	PHY_ADDR2
CS3	PHY_ADDR3
CS4	PHY_ADDR4
CS5	PHY_ADDR5
CS6	PHY_ADDR6
CS7	PHY_ADDR7
CS8	PHY_ADDR8
CS9	PHY_ADDR9
CS10	PHY_ADDR10
CS11	PHY_ADDR11
CS12	PHY_ADDR12
CS13	PHY_ADDR13
CS14	PHY_ADDR14
CS15	PHY_ADDR15
CS16	PHY_ADDR16
CS17	PHY_ADDR17
CS18	PHY_ADDR18
CS19	PHY_ADDR19
CS20	PHY_ADDR20
CS21	PHY_ADDR21
CS22	PHY_ADDR22
CS23	PHY_ADDR23
CS24	PHY_ADDR24
CS25	PHY_ADDR25
CS26	PHY_ADDR26
CS27	PHY_ADDR27
CS28	PHY_ADDR28
CS29	PHY_ADDR29
CS30	PHY_ADDR30
CS31	PHY_ADDR31
CS32	PHY_ADDR32
CS33	PHY_ADDR33
CS34	PHY_ADDR34
CS35	PHY_ADDR35
CS36	PHY_ADDR36
CS37	PHY_ADDR37
CS38	PHY_ADDR38
CS39	PHY_ADDR39
CS40	PHY_ADDR40
CS41	PHY_ADDR41
CS42	PHY_ADDR42
CS43	PHY_ADDR43
CS44	PHY_ADDR44
CS45	PHY_ADDR45
CS46	PHY_ADDR46
CS47	PHY_ADDR47
CS48	PHY_ADDR48
CS49	PHY_ADDR49
CS50	PHY_ADDR50
CS51	PHY_ADDR51
CS52	PHY_ADDR52
CS53	PHY_ADDR53
CS54	PHY_ADDR54
CS55	PHY_ADDR55
CS56	PHY_ADDR56
CS57	PHY_ADDR57
CS58	PHY_ADDR58
CS59	PHY_ADDR59
CS60	PHY_ADDR60
CS61	PHY_ADDR61
CS62	PHY_ADDR62
CS63	PHY_ADDR63
CS64	PHY_ADDR64
CS65	PHY_ADDR65
CS66	PHY_ADDR66
CS67	PHY_ADDR67
CS68	PHY_ADDR68
CS69	PHY_ADDR69
CS70	PHY_ADDR70
CS71	PHY_ADDR71
CS72	PHY_ADDR72
CS73	PHY_ADDR73
CS74	PHY_ADDR74
CS75	PHY_ADDR75
CS76	PHY_ADDR76
CS77	PHY_ADDR77
CS78	PHY_ADDR78
CS79	PHY_ADDR79
CS80	PHY_ADDR80
CS81	PHY_ADDR81
CS82	PHY_ADDR82
CS83	PHY_ADDR83
CS84	PHY_ADDR84
CS85	PHY_ADDR85
CS86	PHY_ADDR86
CS87	PHY_ADDR87
CS88	PHY_ADDR88
CS89	PHY_ADDR89
CS90	PHY_ADDR90
CS91	PHY_ADDR91
CS92	PHY_ADDR92
CS93	PHY_ADDR93
CS94	PHY_ADDR94
CS95	PHY_ADDR95
CS96	PHY_ADDR96
CS97	PHY_ADDR97
CS98	PHY_ADDR98
CS99	PHY_ADDR99
CS100	PHY_ADDR100

R1	R9	CLR	OUT
1	1	200mV	
1	1	100mV	
1	1	125mV	
1	1	200mV	

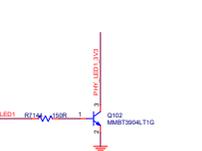
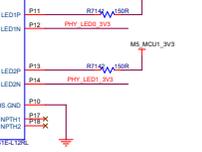
120mA

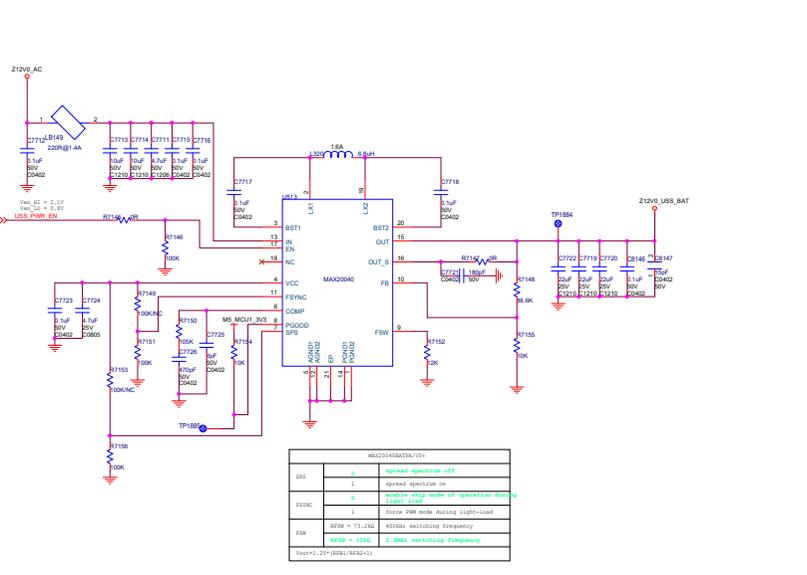
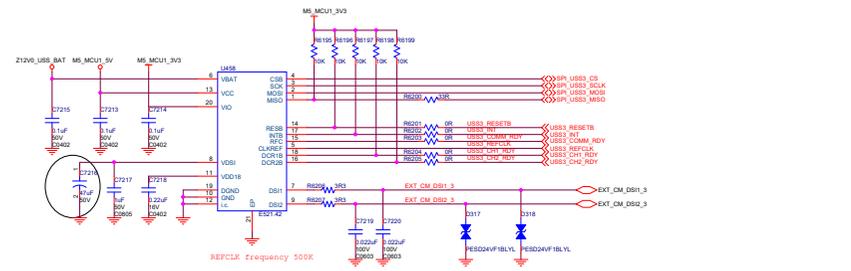
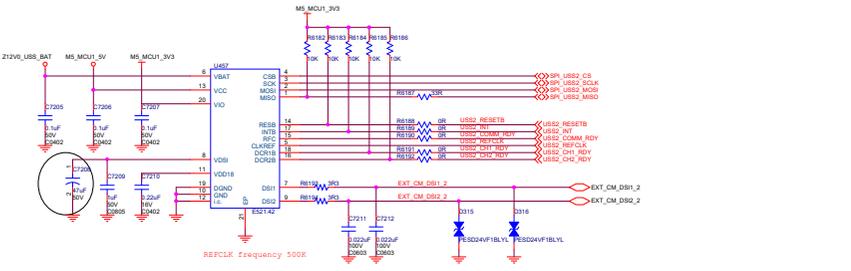
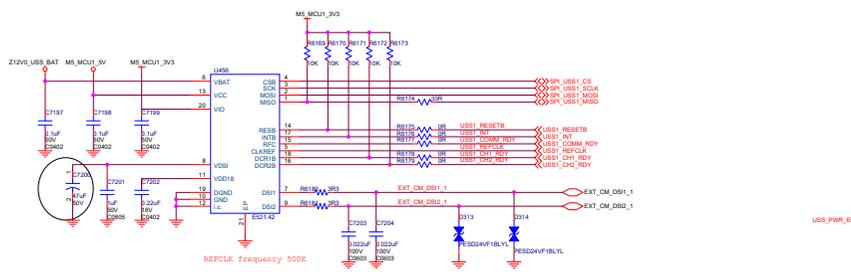


TO EthSW, and Debug RJ45



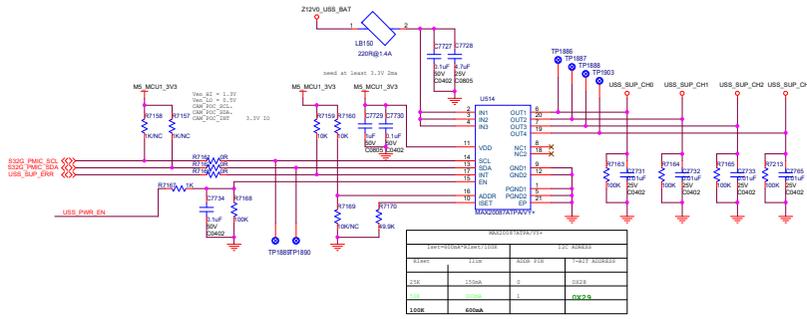
88EA1512:	
CS0	PHY_ADDR0
CS1	PHY_ADDR1
CS2	PHY_ADDR2
CS3	PHY_ADDR3
CS4	PHY_ADDR4
CS5	PHY_ADDR5
CS6	PHY_ADDR6
CS7	PHY_ADDR7
CS8	PHY_ADDR8
CS9	PHY_ADDR9
CS10	PHY_ADDR10
CS11	PHY_ADDR11
CS12	PHY_ADDR12
CS13	PHY_ADDR13
CS14	PHY_ADDR14
CS15	PHY_ADDR15
CS16	PHY_ADDR16
CS17	PHY_ADDR17
CS18	PHY_ADDR18
CS19	PHY_ADDR19
CS20	PHY_ADDR20
CS21	PHY_ADDR21
CS22	PHY_ADDR22
CS23	PHY_ADDR23
CS24	PHY_ADDR24
CS25	PHY_ADDR25
CS26	PHY_ADDR26
CS27	PHY_ADDR27
CS28	PHY_ADDR28
CS29	PHY_ADDR29
CS30	PHY_ADDR30
CS31	PHY_ADDR31
CS32	PHY_ADDR32
CS33	PHY_ADDR33
CS34	PHY_ADDR34
CS35	PHY_ADDR35
CS36	PHY_ADDR36
CS37	PHY_ADDR37
CS38	PHY_ADDR38
CS39	PHY_ADDR39
CS40	PHY_ADDR40
CS41	PHY_ADDR41
CS42	PHY_ADDR42
CS43	PHY_ADDR43
CS44	PHY_ADDR44
CS45	PHY_ADDR45
CS46	PHY_ADDR46
CS47	PHY_ADDR47
CS48	PHY_ADDR48
CS49	PHY_ADDR49
CS50	PHY_ADDR50
CS51	PHY_ADDR51
CS52	PHY_ADDR52
CS53	PHY_ADDR53
CS54	PHY_ADDR54
CS55	PHY_ADDR55
CS56	PHY_ADDR56
CS57	PHY_ADDR57
CS58	PHY_ADDR58
CS59	PHY_ADDR59
CS60	PHY_ADDR60
CS61	PHY_ADDR61
CS62	PHY_ADDR62
CS63	PHY_ADDR63
CS64	PHY_ADDR64
CS65	PHY_ADDR65
CS66	PHY_ADDR66
CS67	PHY_ADDR67
CS68	PHY_ADDR68
CS69	PHY_ADDR69
CS70	PHY_ADDR70
CS71	PHY_ADDR71
CS72	PHY_ADDR72
CS73	PHY_ADDR73
CS74	PHY_ADDR74
CS75	PHY_ADDR75
CS76	PHY_ADDR76
CS77	PHY_ADDR77
CS78	PHY_ADDR78
CS79	PHY_ADDR79
CS80	PHY_ADDR80
CS81	PHY_ADDR81
CS82	PHY_ADDR82
CS83	PHY_ADDR83
CS84	PHY_ADDR84
CS85	PHY_ADDR85
CS86	PHY_ADDR86
CS87	PHY_ADDR87
CS88	PHY_ADDR88
CS89	PHY_ADDR89
CS90	PHY_ADDR90
CS91	PHY_ADDR91
CS92	PHY_ADDR92
CS93	PHY_ADDR93
CS94	PHY_ADDR94
CS95	PHY_ADDR95
CS96	PHY_ADDR96
CS97	PHY_ADDR97
CS98	PHY_ADDR98
CS99	PHY_ADDR99
CS100	PHY_ADDR100





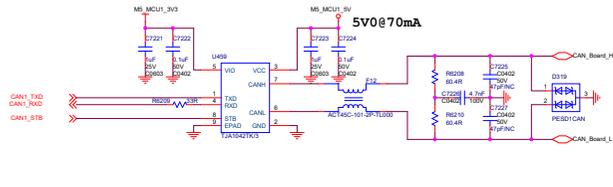
MAX9213(03A)T1700			
225	3	spread spectrum	OFF
226	1	spread spectrum	on
227	0	enable skip mode of operation	skip
228	1	force PWM mode during light-load	off
229	0	400kHz switching frequency	
230	0	3.0MHz switching frequency	

Value: 0,10,0,0,0,0,0,0,0,0

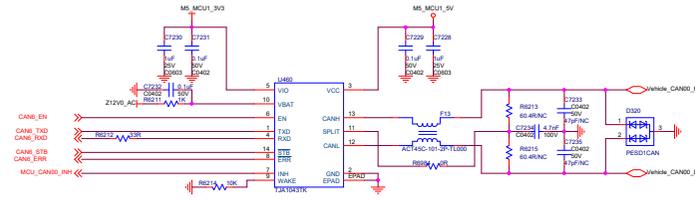


MAX9211(03A)T1711			
400	1	mode	0000
401	1	mode	0000
402	0	mode	0000
403	0	mode	0000

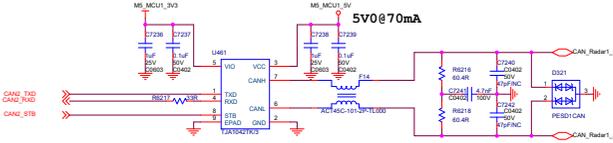
Use VPRE\_3V3 ?



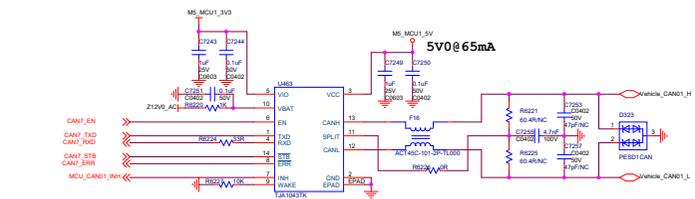
Private\_CAN



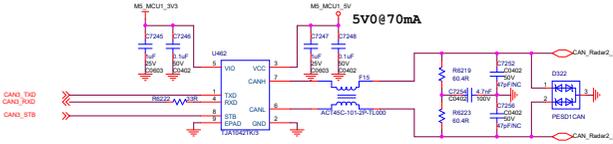
Vehicle CAN00



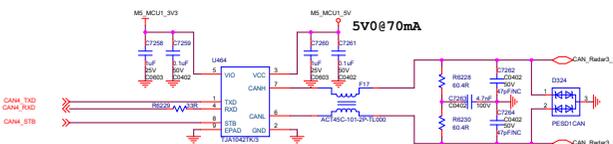
Radar\_CAN1



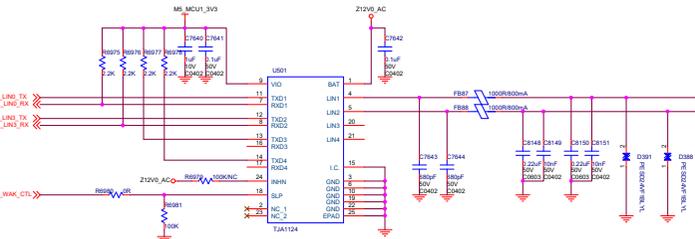
Vehicle CAN01



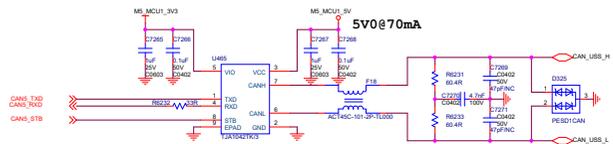
Radar\_CAN2



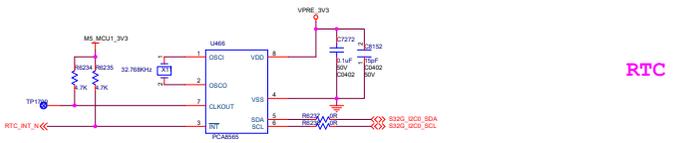
Radar\_CAN3



LIN

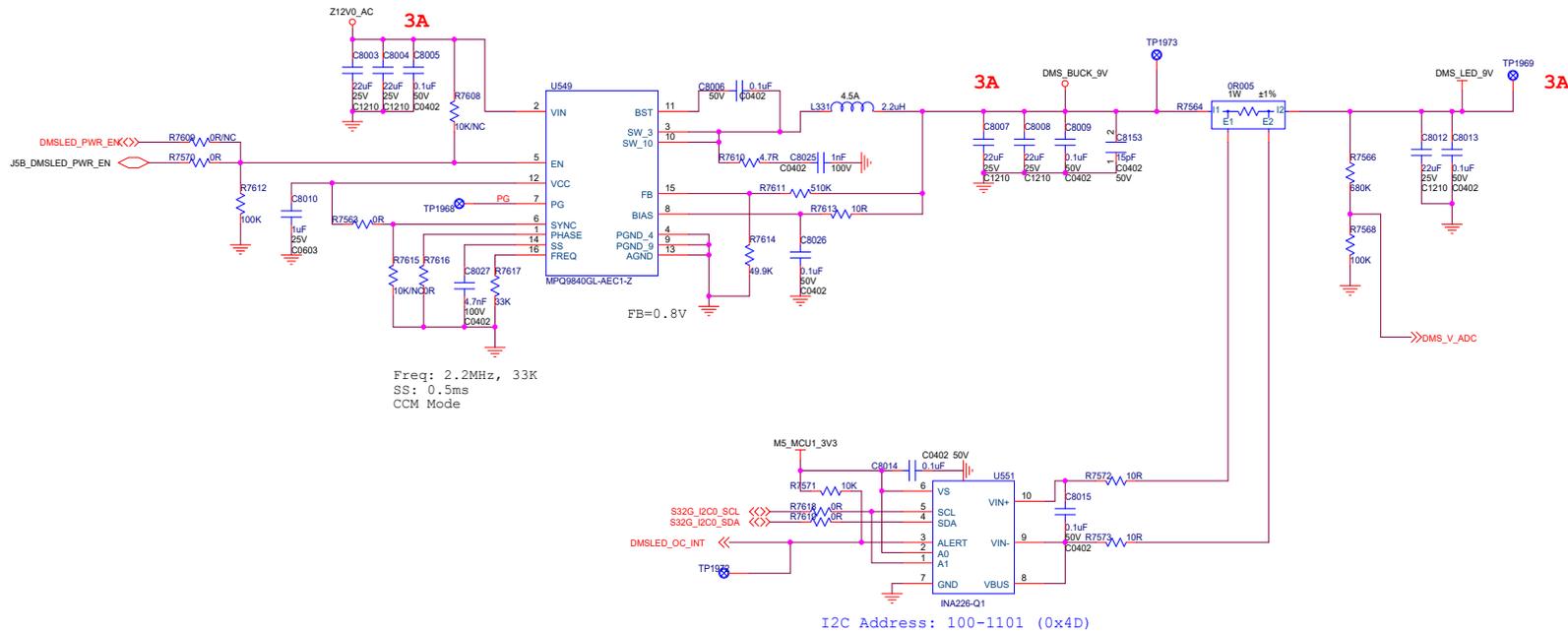


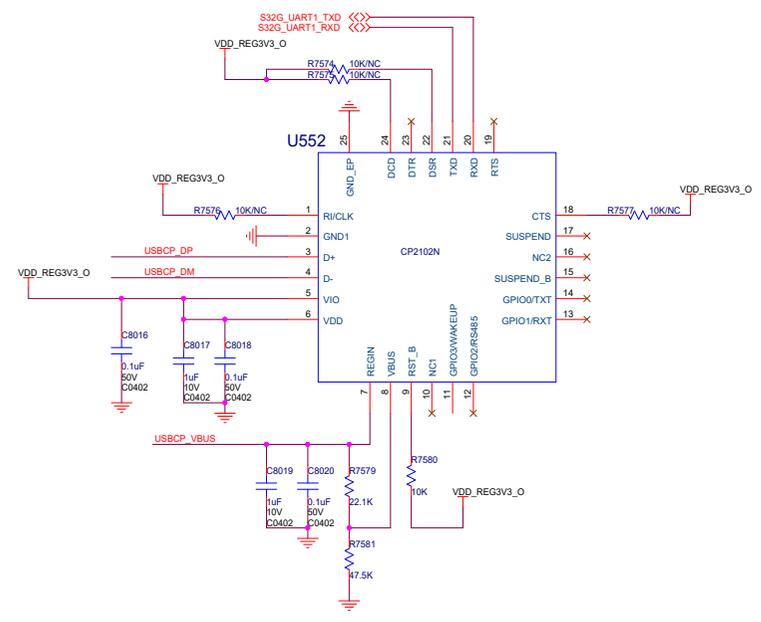
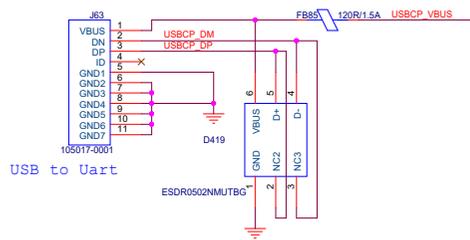
IMU or USS



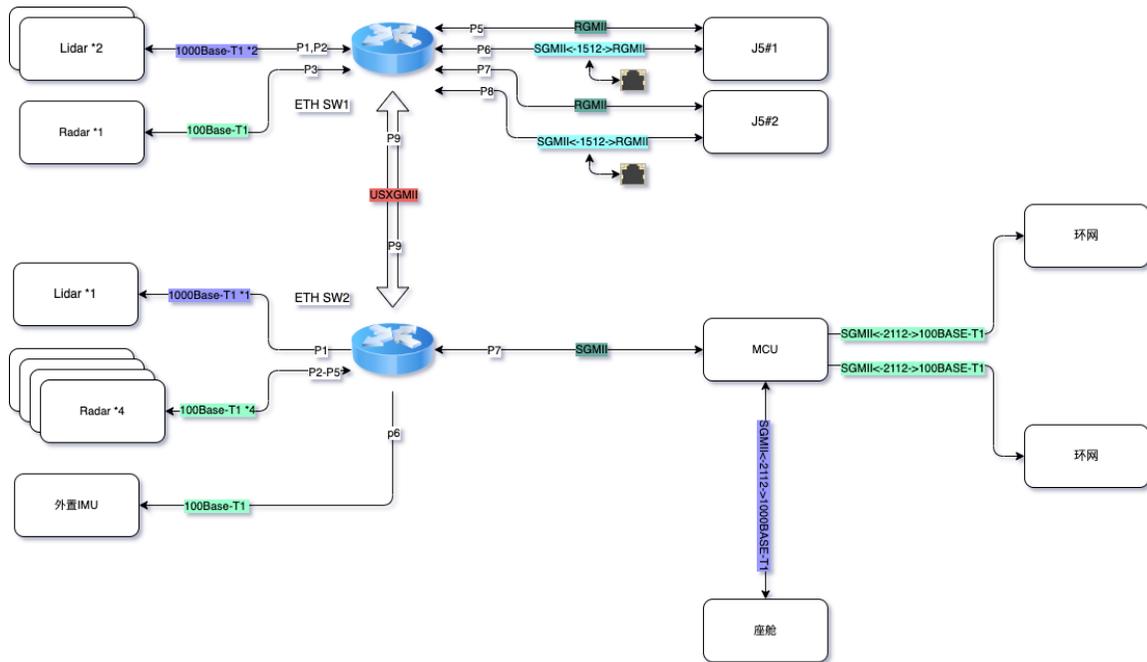
RTC

IO0 address: 0x40 0x43 0x54 0x62  
Title : 0x11





Page Name: 13_Debug_uart	Project: <Title>	Rev: <Rev Code>
Designer:		
Date: Saturday, April 23, 2022		
Sheet: 50 of 68		

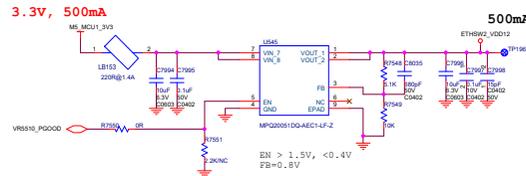
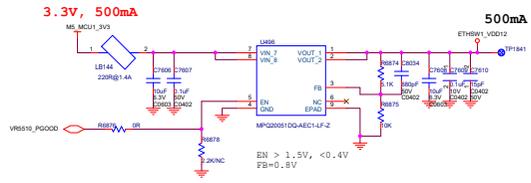
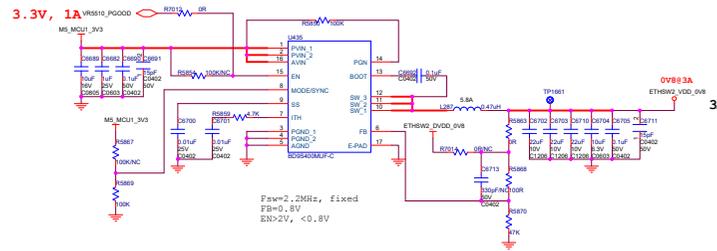
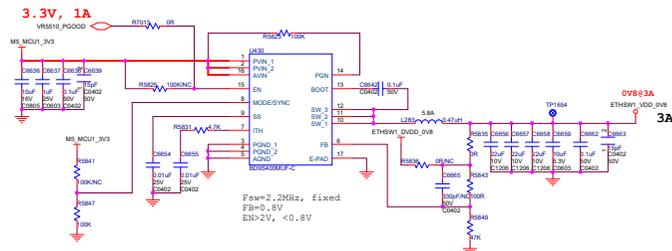


Black for general information  
 Green for notice  
 Red for pending



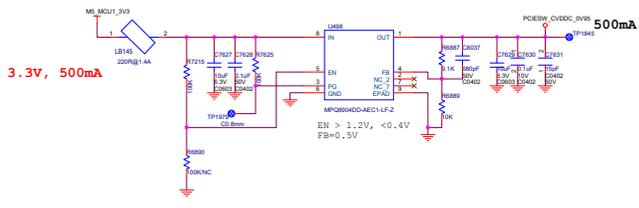
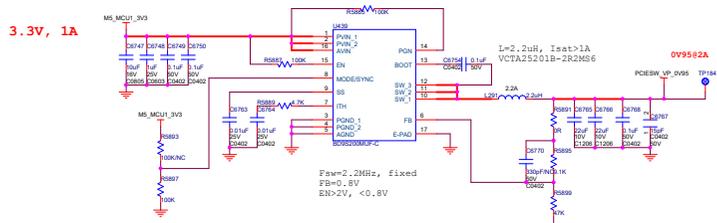
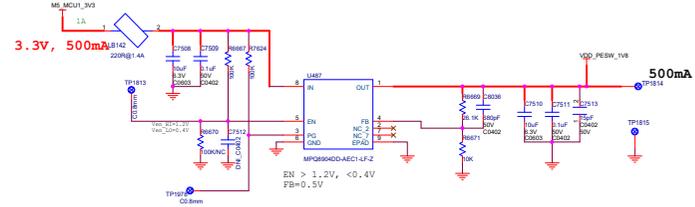
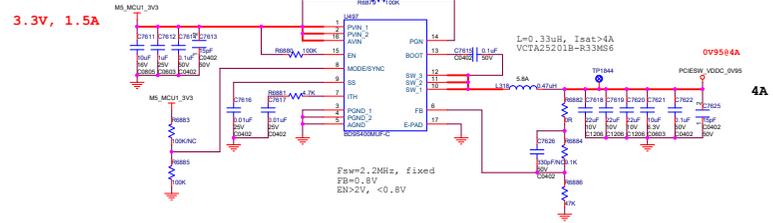
**CONFIDENTIAL**

NAME: 01_ETH_BLOCK	VERSION: <Version>
PROJECT: MATRX05_P3_2XJ5_0428-A	
DESIGNER: Horizon Hardware Team	
DRAWING DATE: Thursday, February 24, 2022	
PAGE: 60	of 69

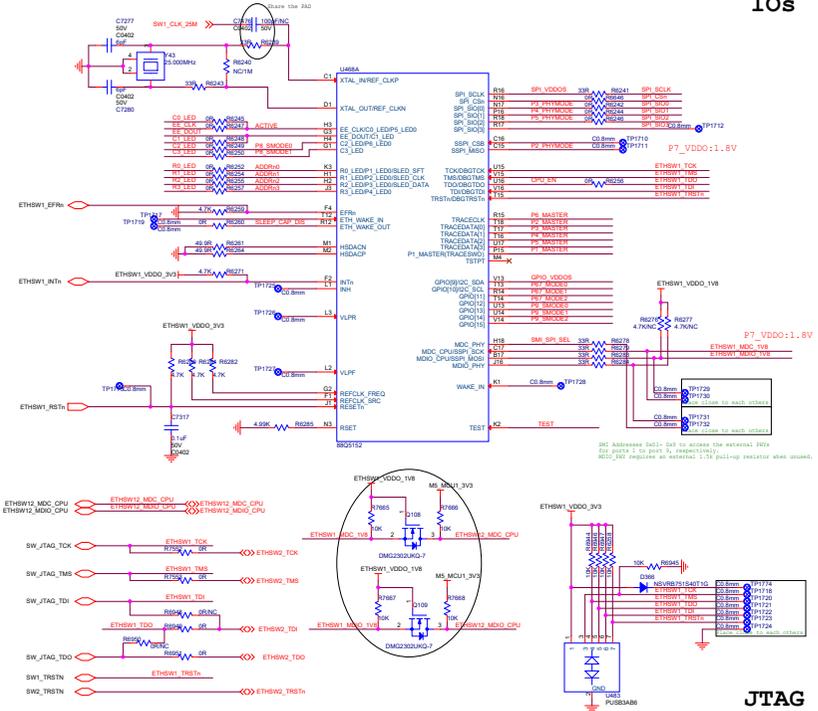


ETH SW power supply

PCIe SW power supply



# IOs



# JTAG

Power Rails	Pin	Voltage
SP1_VDD0	SP1_VDD00	1.2V
SP1_VDD1	SP1_VDD01	1.2V
SP1_VDD2	SP1_VDD02	1.2V
SP1_VDD3	SP1_VDD03	1.2V
SP1_VDD4	SP1_VDD04	1.2V
SP1_VDD5	SP1_VDD05	1.2V
SP1_VDD6	SP1_VDD06	1.2V
SP1_VDD7	SP1_VDD07	1.2V
SP1_VDD8	SP1_VDD08	1.2V
SP1_VDD9	SP1_VDD09	1.2V
SP1_VDD10	SP1_VDD10	1.2V
SP1_VDD11	SP1_VDD11	1.2V
SP1_VDD12	SP1_VDD12	1.2V
SP1_VDD13	SP1_VDD13	1.2V
SP1_VDD14	SP1_VDD14	1.2V
SP1_VDD15	SP1_VDD15	1.2V
SP1_VDD16	SP1_VDD16	1.2V
SP1_VDD17	SP1_VDD17	1.2V
SP1_VDD18	SP1_VDD18	1.2V
SP1_VDD19	SP1_VDD19	1.2V
SP1_VDD20	SP1_VDD20	1.2V
SP1_VDD21	SP1_VDD21	1.2V
SP1_VDD22	SP1_VDD22	1.2V
SP1_VDD23	SP1_VDD23	1.2V
SP1_VDD24	SP1_VDD24	1.2V
SP1_VDD25	SP1_VDD25	1.2V
SP1_VDD26	SP1_VDD26	1.2V
SP1_VDD27	SP1_VDD27	1.2V
SP1_VDD28	SP1_VDD28	1.2V
SP1_VDD29	SP1_VDD29	1.2V
SP1_VDD30	SP1_VDD30	1.2V
SP1_VDD31	SP1_VDD31	1.2V
SP1_VDD32	SP1_VDD32	1.2V
SP1_VDD33	SP1_VDD33	1.2V
SP1_VDD34	SP1_VDD34	1.2V
SP1_VDD35	SP1_VDD35	1.2V
SP1_VDD36	SP1_VDD36	1.2V
SP1_VDD37	SP1_VDD37	1.2V
SP1_VDD38	SP1_VDD38	1.2V
SP1_VDD39	SP1_VDD39	1.2V
SP1_VDD40	SP1_VDD40	1.2V
SP1_VDD41	SP1_VDD41	1.2V
SP1_VDD42	SP1_VDD42	1.2V
SP1_VDD43	SP1_VDD43	1.2V
SP1_VDD44	SP1_VDD44	1.2V
SP1_VDD45	SP1_VDD45	1.2V
SP1_VDD46	SP1_VDD46	1.2V
SP1_VDD47	SP1_VDD47	1.2V
SP1_VDD48	SP1_VDD48	1.2V
SP1_VDD49	SP1_VDD49	1.2V
SP1_VDD50	SP1_VDD50	1.2V
SP1_VDD51	SP1_VDD51	1.2V
SP1_VDD52	SP1_VDD52	1.2V
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SP1_VDD54	SP1_VDD54	1.2V
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SP1_VDD56	SP1_VDD56	1.2V
SP1_VDD57	SP1_VDD57	1.2V
SP1_VDD58	SP1_VDD58	1.2V
SP1_VDD59	SP1_VDD59	1.2V
SP1_VDD60	SP1_VDD60	1.2V
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SP1_VDD66	SP1_VDD66	1.2V
SP1_VDD67	SP1_VDD67	1.2V
SP1_VDD68	SP1_VDD68	1.2V
SP1_VDD69	SP1_VDD69	1.2V
SP1_VDD70	SP1_VDD70	1.2V
SP1_VDD71	SP1_VDD71	1.2V
SP1_VDD72	SP1_VDD72	1.2V
SP1_VDD73	SP1_VDD73	1.2V
SP1_VDD74	SP1_VDD74	1.2V
SP1_VDD75	SP1_VDD75	1.2V
SP1_VDD76	SP1_VDD76	1.2V
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SP1_VDD78	SP1_VDD78	1.2V
SP1_VDD79	SP1_VDD79	1.2V
SP1_VDD80	SP1_VDD80	1.2V
SP1_VDD81	SP1_VDD81	1.2V
SP1_VDD82	SP1_VDD82	1.2V
SP1_VDD83	SP1_VDD83	1.2V
SP1_VDD84	SP1_VDD84	1.2V
SP1_VDD85	SP1_VDD85	1.2V
SP1_VDD86	SP1_VDD86	1.2V
SP1_VDD87	SP1_VDD87	1.2V
SP1_VDD88	SP1_VDD88	1.2V
SP1_VDD89	SP1_VDD89	1.2V
SP1_VDD90	SP1_VDD90	1.2V
SP1_VDD91	SP1_VDD91	1.2V
SP1_VDD92	SP1_VDD92	1.2V
SP1_VDD93	SP1_VDD93	1.2V
SP1_VDD94	SP1_VDD94	1.2V
SP1_VDD95	SP1_VDD95	1.2V
SP1_VDD96	SP1_VDD96	1.2V
SP1_VDD97	SP1_VDD97	1.2V
SP1_VDD98	SP1_VDD98	1.2V
SP1_VDD99	SP1_VDD99	1.2V
SP1_VDD100	SP1_VDD100	1.2V

# CONFIG

Port	Pin	Mode
Port 1	PT_MASTER	PT_MASTER
	PT_SLAVE	PT_SLAVE
Port 2	PT_MASTER	PT_MASTER
	PT_SLAVE	PT_SLAVE
Port 3	PT_MASTER	PT_MASTER
	PT_SLAVE	PT_SLAVE
Port 4	PT_MASTER	PT_MASTER
	PT_SLAVE	PT_SLAVE
Port 5	PT_MASTER	PT_MASTER
	PT_SLAVE	PT_SLAVE
Port 6	PT_MASTER	PT_MASTER
	PT_SLAVE	PT_SLAVE
Port 7	PT_MASTER	PT_MASTER
	PT_SLAVE	PT_SLAVE
Port 8	PT_MASTER	PT_MASTER
	PT_SLAVE	PT_SLAVE
Port 9	PT_MASTER	PT_MASTER
	PT_SLAVE	PT_SLAVE

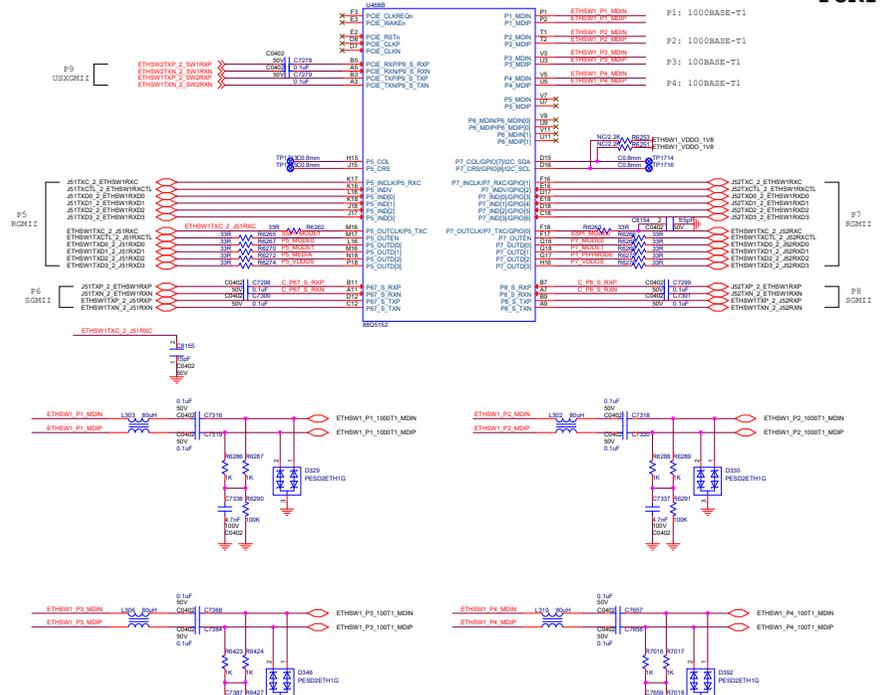
# Flash



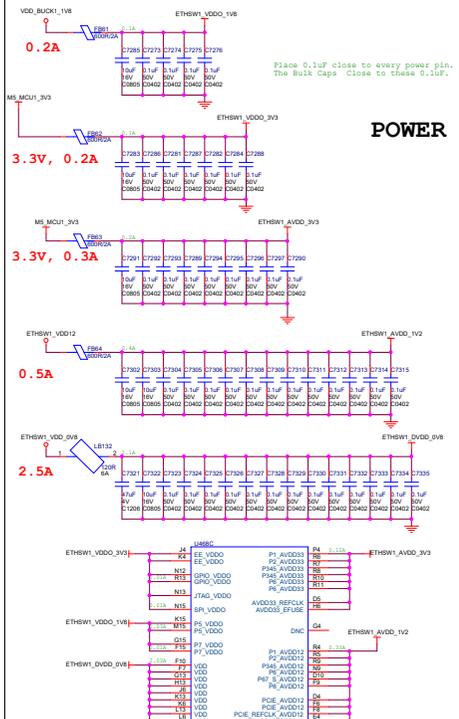
# EEPROM



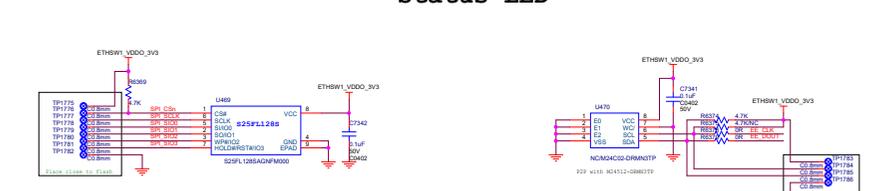
# PORT



# POWER



# Status LED



**CONFIDENTIAL**

NAME: G3\_ETHW1 | VERSION: v1000-0

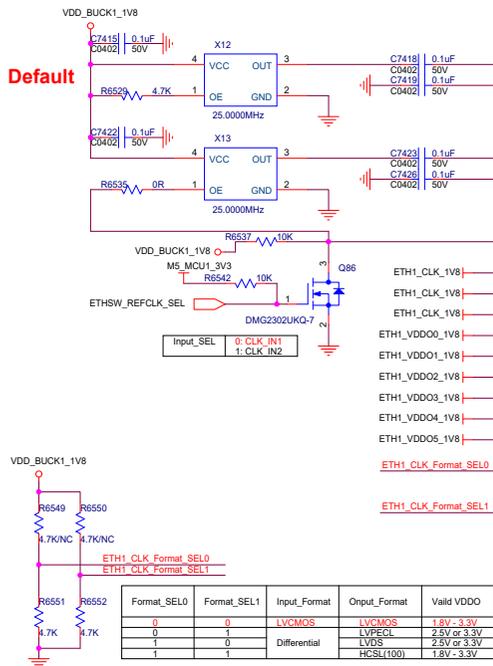
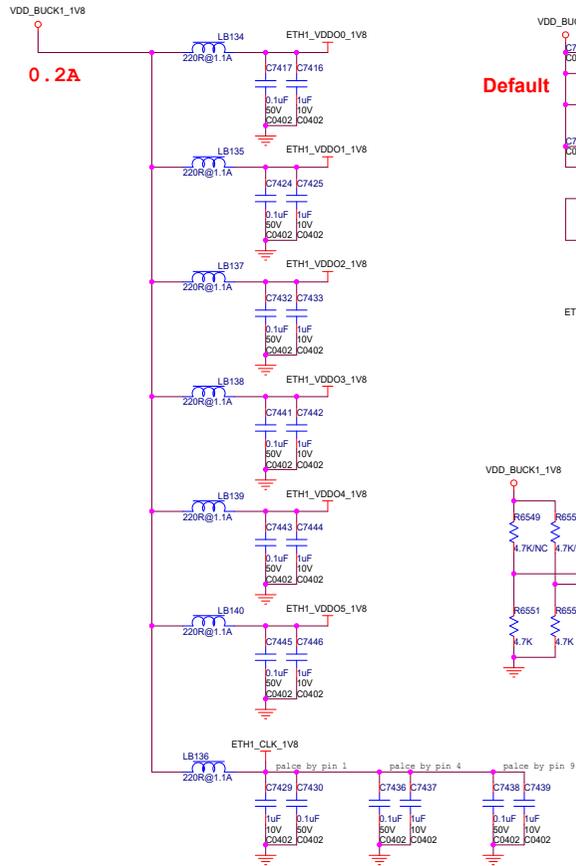
PROJECT: MATROS\_P3\_2x2\_0420A

DESIGNER: Horizon Hardware Team

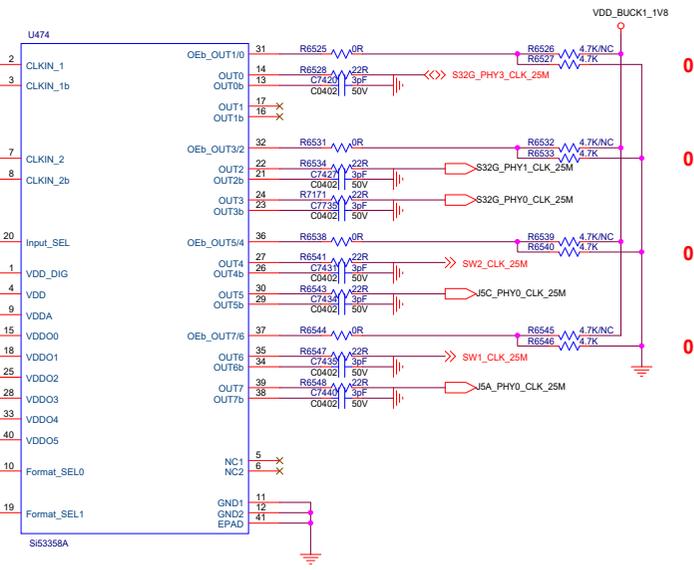
DRAWING DATE: Friday, February 26, 2022

PAGE: 42 of 49



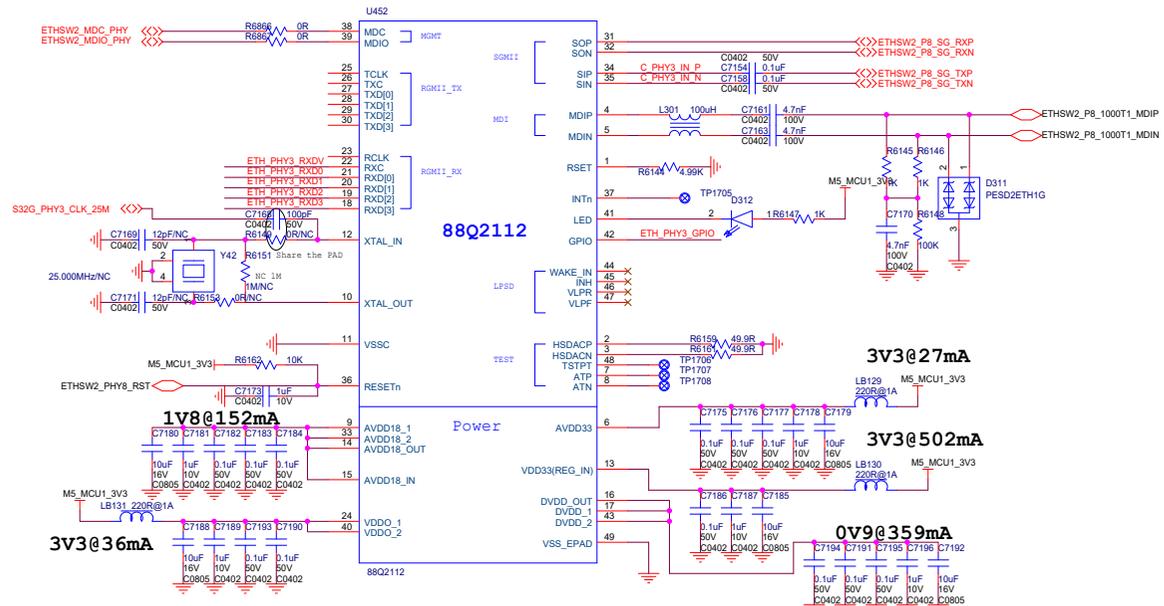


Format_SEL0	Format_SEL1	Input_Format	Onput_Format	Valid VDD0
0	0	LVCMOS	LVCMOS	1.8V - 3.3V
0	1		LVPECL	2.5V or 3.3V
1	0	Differential	LVDS	2.5V or 3.3V
1	1		HCSL(100)	1.8V - 3.3V



**CONFIDENTIAL**

NAME: 05_ETH_CLK	VERSION: v1.0
PROJECT: M5_Board	
DESIGNER: HR-HardWare	
DRAWING DATE: 2021-03-15	
PAGE: 64 of 89	



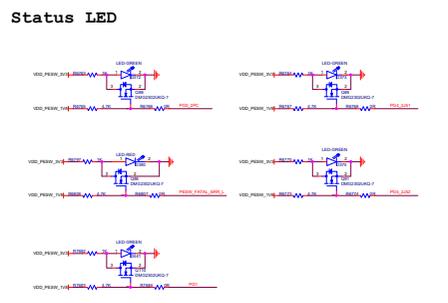
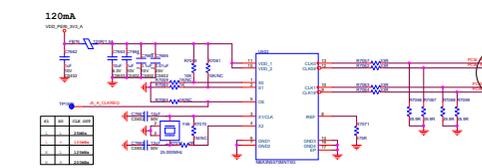
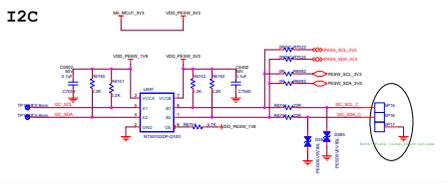
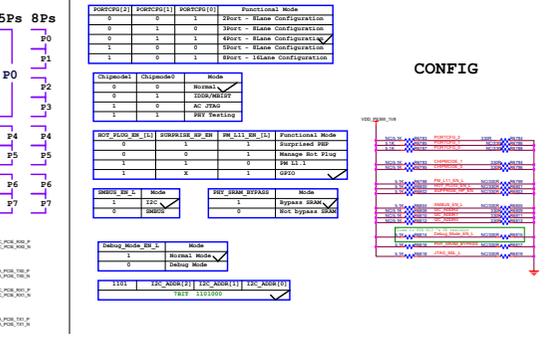
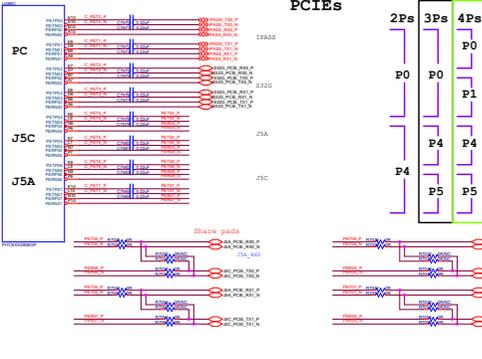
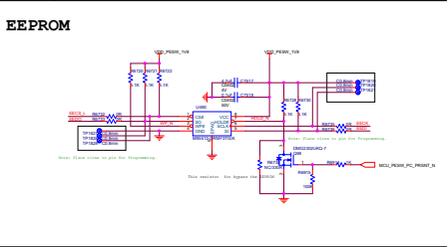
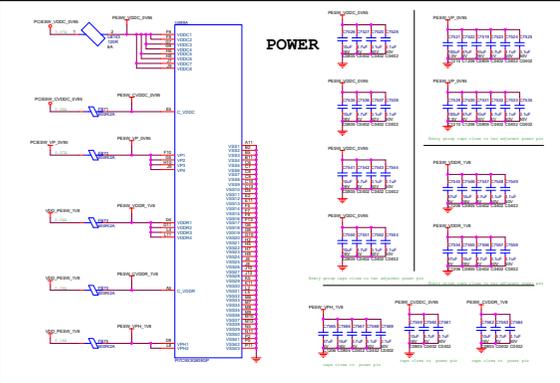
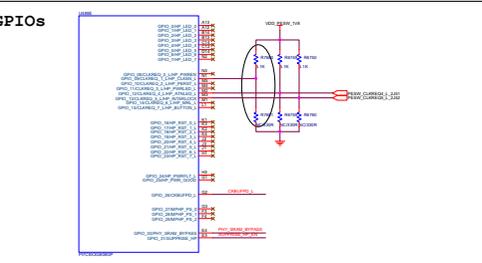
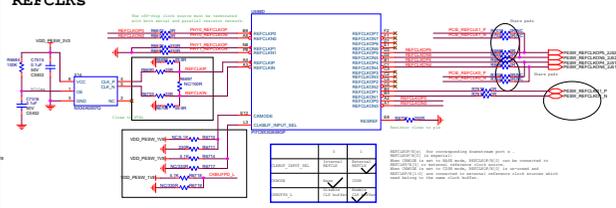
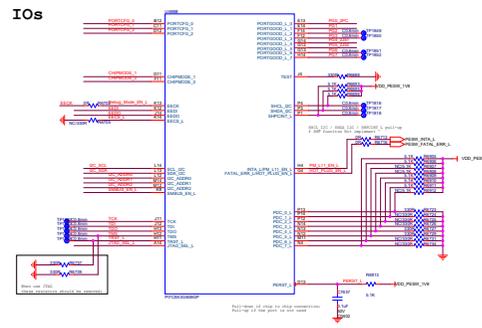
M5\_MCU1\_3V3  
 R8114 4.7K ETH\_PHY3\_GPIO  
 R8118 4.7KNC ETH\_PHY3\_RXD1  
 R8121 4.7K ETH\_PHY3\_RXD0  
 R8125 4.7K ETH\_PHY3\_RXD2  
 R8128 4.7KNC  
 R8134 4.7K ETH\_PHY3\_RXD3  
 R8137 4.7KNC  
 R8142 4.7K ETH\_PHY3\_RXDV

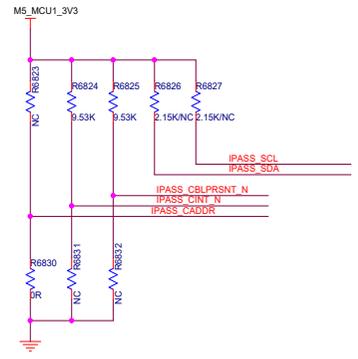
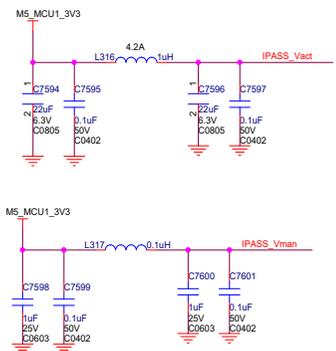
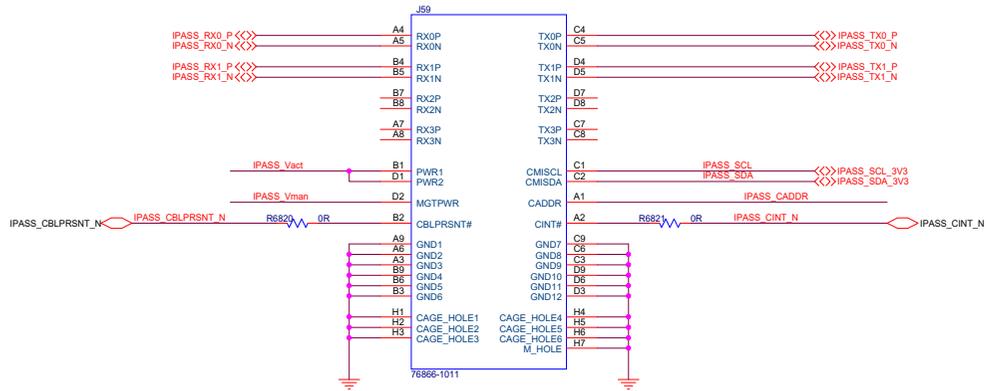
**PHY\_ADDR:101**  
**SGMII, 1000Base-T1, Slave**

**88Q2112:**

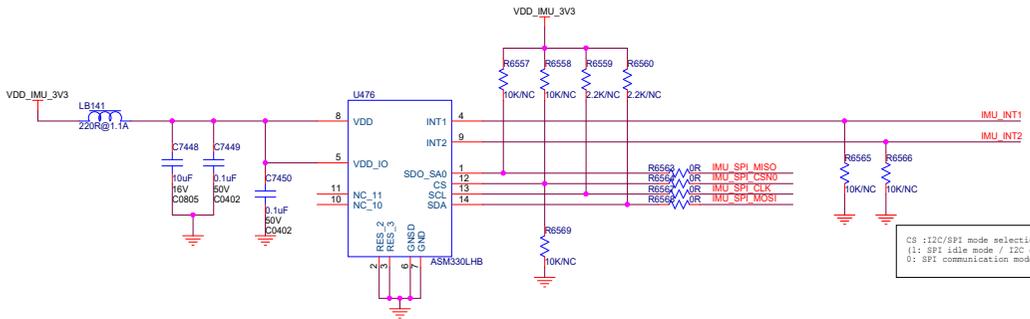
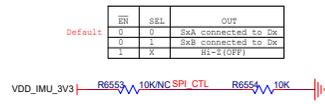
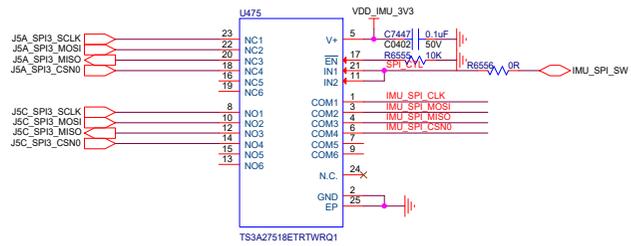
GPIO	PHY_ADDR[0]
RXD[1]	PHY_ADDR[1]
RXD[0]	PHY_ADDR[0]
RXD[3:2]	00:100Base-T1, Master
(88Q2112)	01:100Base-T1, Slave
	10:1000Base-T1, Master
	11:1000Base-T1, Slave
RXCTL	0:RCGMII Delay TX & RX Clock
	1:SGMII







Page Name: 08_PCIE_CONN	Project: <Title>	Rev: <Rev Code>
Designer:		
Date: Thursday, April 28, 2022		
Sheet: 67 of 68		



CS : I2C/SPI mode selection  
 (1: SPI idle mode / I2C communication enabled;  
 0: SPI communication mode / I2C disabled and reset)

